(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 0 421 712 B1

(12) EUROPEAN PATENT SPECIFICATION

(45) Date of publication and mention of the grant of the patent:
14.05.1997 Bulletin 1997/20

(51) Int Cl.6: **H04N 1/40**

(21) Application number: **90310739.9**

(22) Date of filing: **01.10.1990**

(54) Image forming apparatus, and modulating method therein

Bilderzeugungsgerät und Modulationsverfahren

Dispositif pour la formation d'image, et procédé de modulation

(84) Designated Contracting States:
DE FR GB IT

(30) Priority: **02.10.1989 JP 255294/89**
17.10.1989 JP 268227/89
20.11.1989 JP 299732/89

(43) Date of publication of application:
10.04.1991 Bulletin 1991/15

(60) Divisional application: **96202904.7**

(73) Proprietor: **CANON KABUSHIKI KAISHA**
Tokyo (JP)

(72) Inventors:
- **Ojima, Masaki**
  Yokohama-shi, Kanagawa-ken (JP)
- **Ohkubo, Masaharu**
  Yokohama-shi, Kanagawa-ken (JP)
- **Itoh, Michio**
  Hachiohji-shi, Tokyo (JP)
- **Sasame, Hiroshi**
  Yokohama-shi, Kanagawa-ken (JP)
- **Yamada, Hiromichi**
  Yokohama-shi, Kanagawa-ken (JP)
- **Saito, Tetsuo**
  Tokyo (JP)
- **Kashihara, Atsushi**
  Tokyo (JP)
- **Kawana, Takashi**
  Yokohama-shi, Kanagawa-ken (JP)
- **Mano, Hiroshi**
  Tokyo (JP)
- **Seto, Kaoru**
  Chigasaki-shi, Kanagawa-ken (JP)
- **Atobe, Hiroshi**
  Yokohama-shi, Kanagawa-ken (JP)

(74) Representative:
Beresford, Keith Denis Lewis et al
BERESFORD & Co.
2-5 Warwick Court
High Holborn
London WC1R 5DJ (GB)

(56) References cited:
EP-A- 0 080 075
EP-A- 0 104 285
EP-A- 0 234 809
GB-A- 2 196 498
US-A- 4 347 523
US-A- 4 365 202
US-A- 4 415 907
US-A- 4 498 090
US-A- 4 633 222
US-A- 4 679 057
US-A- 4 754 291

- **PATENT ABSTRACTS OF JAPAN, vol. 9, no. 95 (E-310)(1818) 24th April 1985; & JP-A-59 223 070 (CANON K.K.) 14-12-1984**
- **PATENT ABSTRACTS OF JAPAN, vol. 10, no. 184 (E-415)(2240), 27th June 1986; & JP-A-61 30 118 (NEC CORP.) 12-02-1986**
- **PATENT ABSTRACTS OF JAPAN, vol. 6, no. 16 (E-92)(894), 29th January 1982; & JP-A-56 138 328 (CHO LSI GIJUTSU KENKYU KUMIAI) 28-10-1981**
- **PATENT ABSTRACTS OF JAPAN, vol. 12, no. 261 (E-636), July 22, 1988; & JP-A-63 045 973 (CANON INC.) 26-02-1988**
- **PATENT ABSTRACTS OF JAPAN, vol. 13, no. 280 (E-779), July 27, 1989; & JP-A-1 067 030 (YAMAHA CORP.) 13-03-1989**
- **PATENT ABSTRACTS OF JAPAN, vol. 13, no. 381 (E-810), August 23, 1989; & JP-A-1 129 774 (TOSHIBA CORP.) 23-05-1989**
- **PATENT ABSTRACTS OF JAPAN, vol. 8, no. 261 (E-281), November 30, 1984; & JP-A-59 131 225 (YENERARU K.K.) 28-07-1984**

EP 0 421 712 B1

Printed by Jouve, 75001 PARIS (FR)

(Cont. next page)

- PATENT ABSTRACTS OF JAPAN, vol. 9, no. 270 (E-353), October 26,1985; & JP-A-60 116-220 (MATSUSHITA DENKI SANGYO K.K.) 28-11-1983
- PATENT ABSTRACTS OF JAPAN, vol. 9, no. 251 (E-348), October 8, 1985; & JP-A-60 100 831 (SONY K.K.) 04-06-1985

Description

This invention relates to an image forming apparatus, particularly an image forming apparatus to which multivalued image data is inputted for forming the data into a visible image which includes half tones, and a modulating method therein.

A pulse-width modulating (PWM) method is known as a technique through which half tones are expressed based upon an inputted multivalued image signal.

According to the conventional PWM method, a multivalued input signal is converted into an analog signal which is then compared with an analog waveform (usually a sawtooth waveform) used for comparison purposes, thereby converting the input signal into a pulse-width modulated signal.

This conventional PWM method will now be described with reference to the timing chart shown in Fig. 12.

In the conventional method, as shown in Fig. 12, an inputted multivalued input image signal VDO is converted into an analog voltage waveform by a D/A converter using an image clock signal VCLK transmitted in synchronism with the input image signal VDO, thereby producing an analog image signal AV.

A sawtooth waveform SAW for comparison purposes generated by an appropriate method and the analog image signal AV are compared by a comparator. If the voltage of the analog image signal AV is greater than the sawtooth waveform SAW for comparison, then an output signal OPD of the above-mentioned comparator is turned "ON". On the other hand, if the voltage of the analog image signal AV is less than the sawtooth waveform SAW for comparison, then the output signal OPD of the above-mentioned comparator is turned "OFF". As a result, the inputted multivalued input image signal VDO is converted into a PWM signal to produce the corresponding recording image signal.

However, with the conventional PWM method of this kind, unstable operation frequently occurs owing to noise and fluctuation of a reference potential for dealing with the analog signal. This makes it difficult to perform a stable conversion to a PWM signal.

Accordingly, an example of an expedient to solve this problem is a method in which the input image signal VDO is compared in the form of a digital signal without being converting into an analog signal. This method is implemented by a circuit having a construction of the kind shown in Fig. 13.

In Fig. 13, a master clock signal CLK is assumed to have a frequency that is n times that of the input image signal VDO.

The input image signal VDO is obtained in a latch circuit 21 in synchronism with an image clock signal VCLK obtained by frequency-dividing a master clock signal CLK using a frequency divider 23. The image signal VDO enters a comparator 24.

Numeral 26 denotes a comparison signal generator which generates a comparison signal CMPD for comparison with the input image signal VDO whenever the master clock signal CLK is produced. The number of bits in the signal CMPD corresponds to the number of bits in the input image signal VDO. The comparison signal CMPD outputted by the comparison signal generator 26 is synchronized with the master clock signal CLK in a latch before being inputted to the comparator 24.

The comparator 24 compares the level of the input image signal VDO from latch 21 and the level of the comparison signal CMPD from the latch 25, and the result of the comparison is outputted as the output image signal OPD. When VDO > CMPD holds, the comparator 24 turns the output image signal "ON". This signal serves as the recording signal.

The comparison signal CMPD enters the comparator 24 n times while one input image signal VDO is being applied to this comparator. Consequently, the output image signal OPD is a PWM signal having n times the amount of information possessed by the signal VDO.

Fig. 14 shows a time chart associated with the above-described circuit arrangement for a case where the input image signal VDO is a six-bit signal, n is four and an up/down counter is used as the comparison signal generator 26.

The up/down counter produces a level value obtained by adding or subtracting a predetermined value to or from the immediately preceding level value whenever the master clock signal is generated. The counter has upper- and lower-limit values decided for it. Subtraction starts when the upper-limit value is reached as a result of addition, and addition starts when the lower-limit value is reached as a result of subtraction. This operation is performed repeatedly to produce a pseudo-sawtooth waveform. With this method, items of data are compared with each other so there is no danger of unstable operation of the analog kind.

In the example of the prior art described above, however, the minimum pulse width of the output image signal OPD is decided by the frequency of the master clock CLK, and this is accompanied by a limitation upon the number of tones.

In order to increase the number of tones, the frequency of the master clock should be raised. However, electronic circuit elements have a limit upon their operating frequency, and therefore the upper limit of the usable frequency is determined by the electronic circuit elements employed. As a consequence, a PWM conversion having a high number of tones is difficult to carry out.

In general, high-frequency oscillators and high-speed electronic circuit elements having a high operating frequency limit are expensive, and it is uneconomical to construct all of the circuitry using high-frequency elements merely for the purpose of a high tonality PWM conversion.

A pulse-width modulating circuit is used in such image forming apparatus as laser-beam printers and LED

printers.

Fig. 15 is a circuit diagram of a pulse-width modulating circuit in a conventional image forming apparatus, and Fig 16 is an operation timing chart associated with the circuit of Fig. 15.

Four-bit multivalued image data received from external equipment (not shown) such as a host computer or scanner is loaded in a counter 61 at the leading edge of an image clock signal. The counter 61 is successively counted down by a count clock signal outputted by a count clock generator 62. When the counter output becomes zero, the counter 61 outputs a carry signal. In response, the Q output of a J-K flip-flop 63 is set at the leading edge of the image clock signal. The Q output is reset by generation of the carry signal. This output of the flip-flop 63 is a pulse-width modulated signal. This pulse-width modulated signal enters a laser driver circuit (not illustrated) to turn a laser element on and off, thereby sensitizing a photosensitive drum (not shown) so that half-tone printing may be performed using an electrophotographic technique.

However, in order to express a n-tone density using the conventional method described above, the count clock signal is required to have a frequency that is n times the frequency of the image clock signal. For example, if the image clock signal has a frequency of 1 MHz, a count clock signal having a frequency of 256 MHz is required in order to express 256 tones by an eight-bit multivalued image signal. This means that it is necessary to use a high-speed device such as costly ECL (emitter-coupled logic). Another problem is that radiation noise tends to be produced owing to the high-speed operation.

In a case where a half-tone image is outputted by a laser-beam printer employing electrophotography, a method is employed in which screen or dither processing or image processing such as pulse-width modulation is performed by a host computer, which has a data generating source, or a controller, etc., and binary-coded data is inputted to a printer engine section (printer).

In order to deal with the binary-coded data in accordance with this method, a high-efficiency, half-tone data transfer is performed by transfer data compression or the like. On the other hand, with regard to the depth direction of density, it is difficult to obtain the desired stabilized tones, despite the fact that the host computer or controller transmits the same half-tone image data, owing to a delay in the data transmission line, the conditions of the electrophotographic process and differences among equipment.

Furthermore, when different printers are employed using the same host computer or controller, etc., the fact that the correspondence between dither patterns and density differs depending upon the printer means that the host computer or controller requires density correction tables the number of which is equivalent to the number of printers connected. These tables conform to the printers used. A problem that arises in that it is difficult to achieve compatibility with the printers.

A method is available in which image data having tones, such as a document, is read in by an image reader and developed into a dot image to provide each dot with a value in the thickness direction. Figs. 17 (a), (b) are diagrams illustrating the input/output characteristics of a CCD. In a case where a CCD sensor or the like is used as the image input section of the image reader, the density information possessed by the original image is converted into substantially linear voltage information proportional to the light reflected from the original image, as shown in Fig. 23(a). Since the voltage information possesses a logarithmic relation with respect to density [Fig. 17 (b)], this signal is subjected to a correction (a γ correction) in the reader section. However, the image undergoes a major change depending upon the extent of the correction.

In addition, depending upon the model type, the host computer connected possesses various fonts employed by the particular manufacturer. Some host computers tend to express characters boldly, while others express characters more finely.

Thus, there are a large number of varying factors for reproducing image information. As a result, when a single system is constructed from such components as a reader, a host computer and a printer, various problems arise. For example, the obtained image may be too faint overall and characters may appear too fine. Conversely, the overall image may be too dark and the characters distorted. In extreme cases, characters appear fine and photographs or graphics appear distorted and without tone. Conversely, characters become too bold to be legible while photographs and graphics appear too faint.

A method that has been proposed to solve these problems involves controlling the exposure time per dot of the exposing beam by pulse-width modulation (PWM), thereby performing the equivalent of density modulation. Attempts have been made to overcome the foregoing problems by subdividing the density-modulation steps in order to perform more faithful modulation of density.

However, in order to subdivide the density modulation steps, there is a great increase in the amount of processing performed by the pulse-width modulating section (especially the D/A converter contained in the PWM section). Furthermore, in the method of controlling exposure time per dot of the exposing beam by PWM, a variance in pulse width occurs in a region where pulse width is very small. As a consequence, the printing operation for low density becomes unstable.

A concern of the present invention is to provide a simply constructed, inexpensive image forming apparatus, and a modulating method therein, in which it is possible to form a highly toned image.

Another concern of the present invention is to provide an image signal modulating apparatus and method, in which a signal for subdividing one period of a clock is

formed and a highly toned image signal is produced.

A further concern of the present invention is to provide a pulse-width modulating circuit capable of performing faithful pulse-width modulation even without using a count clock signal having a high frequency.

US-A-4,347,523 discloses a pulse-width modulating method in which a fundamental pulse width modulation signal output as a comparison result is delayed to provide a plurality of different delayed pulse width modulation signals. However the disclosure of this specification does not solve the above mentioned problems and uses a high frequency clock signal for counting.

In accordance with the present invention there is provided an image signal modulating device as set out in claim 1 and a method of generating a pulse width modulated signal as set out in claim 15.

An embodiment of the present invention provides an image forming apparatus capable of obtaining an excellent half-tone image at a high or low density.

Embodiments of the present invention will now be described with reference to the accompanying drawings in which:

Fig. 1 is a block diagram illustrating a first embodiment of the present invention;
Fig. 2 is a diagram showing the detailed construction of a delay circuit shown in Fig. 1;
Fig. 3 is a diagram showing the detailed construction of a changeover circuit shown in Fig. 1;
Fig. 4 is an operation timing chart of the present embodiment;
Fig. 5 is a block diagram illustrating a second embodiment of the present invention;
Fig. 6 is a diagram showing the ratios of conversion signals D1 through D4 with respect to one pixel of an input image signal of the second embodiment;
Fig. 7 is a diagram illustrating the state of multiple-tone density realization by the conversion signals D1 - D4 shown in Fig. 6;
Fig. 8 is a diagram showing the relationship between input image signals and output conversion signals D1 - D4 from a ROM in the second embodiment of the invention;
Fig. 9 is a diagram showing the detailed construction of a delay circuit shown in Fig. 5;
Fig. 10 is a diagram showing the detailed construction of a changeover circuit shown in Fig. 5;
Fig. 11 is an operation timing chart of the second embodiment;
Fig. 12 is a diagram for describing analog PWM according to the prior art;
Fig. 13 is a block diagram of digital PWM according to the prior art;
Fig. 14 is a timing chart of the digital PWM of Fig. 13;
Fig. 15 is a circuit diagram showing a pulse-width modulating circuit of a conventional image forming apparatus;
Fig. 16 is an operation timing chart associated with the circuit shown in Fig. 15;
Fig. 17 (a) is a diagram showing the relationship between the output voltage of a CCD and the quantity of light reflected form an original; and
Fig. 17 (b) is a diagram showing the relationship between the output voltage of a CCD and the density of an original

Fig. 1 is a block diagram of an embodiment according to the present invention. This embodiment will now be described in detail with reference to Fig. 1.

In this embodiment, an eight-bit input image signal is pulse-width modulated into an output signal OPD whose minimum pulse width is 1/4 the period of the input image signal VDO. According to this embodiment, a master clock CLK has a frequency the same as that of the input signal VDO.

The eight-bit input image signal VDO is split into two paths by a demultiplexer 1. One path enters a latch I 2 and the other enters a latch II 3. These latch circuits are synchronized by respective clocks DCLK 1, DCLK 2 formed from the master clock CLK by a delay circuit 10. The input image signals thus synchronized by the latches I 2, II 3 respectively enter comparators I 4, II 5 as signals DVDO1, DVDO2.

The construction of the delay circuit 10 is shown in Fig. 2. As illustrated in Fig. 2, the delay circuit 10 outputs the master clock CLK intact as DCLK1 and outputs the signal DCLK2 obtained by applying a 90° phase delay to the master clock CLK. The phase delay is applied by a delay element 16.

The clocks DCLK1, DCLK2 from the delay circuit 10 enter an exclusive-OR (EX-OR) gate 11, which produces a switching clock SCLK1 the period whereof is 1/2 that of the master clock CLK. The clock SCLK1 is inverted by an inverted (NOT) circuit 12, whereby a switching clock SCKL2 is produced. The clock SCLK1 enters an up/down counter I 8, a latch V 13 and a changeover circuit 15, and the clock SCLK2 enters an up/down counter I 29, a latch VI 14 and the changeover circuit 15.

The output of the up/down counter I 8 is counted up or down whenever the clock SCLK1 enters the counter, the output is synchronized with SCLK1 in the latch III 6 and is then delivered to a comparator I 4 as a comparison signal CMPD1.

The up/down counter II 9 and latch IV 7 operate in a similar manner to produce a comparison signal CMPD2 based on SCLK2. The signal CMPD2 is delivered to a comparator II 5.

Thus, as described above, the image data DVDO1 and the comparison signal CMPD1 enter the comparator I 4, in which the two are compared. The output D1' of the comparator 4 becomes logical "1" only when the relation DVDO1 ≥ CMPD1 holds. Similarly, the image data DVDO2 and the comparison signal CMPD2 enter the comparator II 5, and output D2' of the comparator 5 becomes logical "1" only when the relation DVDO2 ≥ CMPD2 holds.

The items of image data D1', D2' enter the latches V 13, VI 14, respectively, where they are synchronized with the respective switching signals SCLK1, SCLK2 and outputted as image data D1, D2. The items of image data D1, D2 enter a changeover circuit 15 where they are alternately selected in successive fashion based on the switching clock signals SCLK1, SCLK2. The successively selected items of data are outputted as serial output image data OPD.

The details of the changeover circuit 15 are shown in Fig. 3.

As shown in Fig. 3, the changeover circuit 15 comprises a J-K flip-flop 17, AND gates 18, 19, and an OR gate 20.

The J-K flip-flop 17 is set by the leading edge of the switching clock SCLK1, and the J-K flip-flop 17 is reset by the leading edge of the switching clock SCLK2. As a result, the AND gate 19 is opened and the AND gate 18 closed at the timing of the leading edge of signal SCLK1, and the AND gate 18 is opened and the AND gate 19 closed at the timing of the leading edge of signal SCLK2. Consequently, when the signal SCLK2 rises, the image data D1 is outputted as the output image data OPD, and when the signal SCLK1 rises, the image data D2 is outputted as the output image data OPD. In other words, the circuit arrangement is such that the serial image data OPD is delivered in an order decided by the latching of the latches V 13, VI 14.

The operation timing of this embodiment is as shown in Fig. 4.

If the frequency of the input image signal VDO in this embodiment is 7 MHz, the signals SCLK1, SCLK2 will have a frequency of 14 MHz and the operating frequency of each circuit element in the changeover circuit 15 will be 28 MHz.

Accordingly, it will suffice to use high-speed operating elements solely for the elements constituting the changeover circuit 15, and the EX-OR gate 11 and inverter circuit 13, which are the circuit elements for producing SCLK1, SCLK2 serving as the control signals of the changeover circuit 15. The other elements need only have a maximum operating frequency on the order of 20 MHz.

It should be noted that the delay clocks SCLK1, SCLK2 which control the output of the image data D1, D2 require to be selected to have frequency which will prevent initial instability of the leading edges of the image data D1, D2.

In this embodiment, the pulse-width modulating signal is converted by the digital comparator which compares the image signal delayed and the comparison signal. However, it may be converted by comparing the image signal and the comparison signal delayed.

[Second Embodiment]

A second embodiment of the invention is illustrated in Fig. 5.

In the second embodiment, one period of the eight-bit input image signal VDO is divided by four to perform pulse-width modulation, just as in the first embodiment described above. However, in the second embodiment, the signal for pulse-width modulation is not divided equally. Instead, weighting is performed by suitably adjusting the delay time of a delay clock DCLK, and the number of tones per input image signal is made 16.

In Fig. 5, the eight-bit input image signal VDO is synchronized with the master clock CLK by a latch I 27, after which the signal is inputted to a VDO/address data converting circuit 28. The VDO/address data converting circuit 28 modifies the density level value of the input image signal VDO and makes a conversion to address data AD for accessing image data stored in a ROM 29.

The ROM 29 outputs four-bit image data VD from a storage area corresponding to this address data. The four-bit image data VD read out of the ROM 29 enters a latch II 30 to be synchronized with the master clock CLK again. The image data VD enters a changeover circuit 32 as four binary parallel signals D1, D2, D3, D4 starting from the largest digit.

The relationship between the input image signal VDO and the image data VD (D1 - D4) read out of the ROM 29 will now be described.

In this embodiment, one pixel of the input image signal VDO is divided so that the ratios shown in Fig. 6 will be established. The items of image data D1 - D4 are assigned to these divided pixels of different size. If each divided pixel is printed when the value of the assigned image data is "1", then combining the items of image data D1 - D4 will make it possible to express 16-tones of density per one pixel of VDO.

In general, it is desired that actual image density and the density level value of the image data VD be proportionally related. However, this depends greatly upon the way in which the pixel is divided. In the present embodimgnt, dividing the pixel in the manner shown in Fig. 6 is for the purpose of approaching this proportional relationship.

If possible density level values D based on the combination of image data D1 - D4 are expressed by assigning numbers of 0 to 15 starting from the smallest value, and if S denotes the percentage of the recording area which a certain density level value occupies in one pixel of VDO, the relationship between D and S can be expressed as a fairly good proportional relationship of the kind shown in Fig. 7.

In the VDO/address data converting circuit 28 and ROM 29, the arrangement is such that VD (D1 - D4) shown in Fig. 8 is outputted from the ROM 29 with respect to the density level value of the input image signal VDO in order that the 16-tone VD shown in Figs. 6, 7 is outputted with respect to the input signal VDO.

On the basis of delay clocks DCLK1 - DCLK4 from a delay circuit 31, a changeover circuit 32 successively produces the output OPD one bit at a time starting from the most significant bit of the image data VD within one

period of the input image signal.

The details of the delay circuit 31 are shown in Fig. 9.

As shown in Fig. 9, the delay circuit 31 comprises delay elements I 33 through III 35. The delay element I 33 delays its input signal by 136.8° (38% of one cycle), the delay element II 34 delays its input signal by 54° (15% of one cycle), and the delay element III 35 delays its input signal by 72° (20% of one cycle). As a result, the delay circuit 31 successively delays the master clock CLK applied thereto, thereby producing the delay clocks DCLK1 - DCLK4, among which DCLK2 through DCLK4 each have a phase different from that of the master clock CLK.

More specifically, DCLK1 is in phase with the master clock CLK, DCLK2 is delayed by 136.8°, DCLK3 is delayed by 190.8°, and DCLK4 is delayed by 262.8°.

The four delay clocks DCLK1 - DCLK4 produced are outputted to the changeover circuit 32. The details of the changeover circuit 32 are shown in Fig. 10.

The changeover circuit 32 is adapted to convert (pulse-width modulate) the four-bit parallel data D1 - D4 from the latch II 30 into a serial pulse-width signal by delay clocks DCLK1 through DCLK4. The delay clock DCLK1 inputted to the changeover circuit 32 places a J-K flip-flop 36 in the set state at the leading edge of the signal, thereby opening an AND gate 40 so that the image data D1 is delivered as the output signal ODP through an OR gate 44. Next, when the delay clock DCLK2 rises, the J-K flip-flop 36 is placed in the reset state, thereby clocking the AND gate 40. In other words, the output of the image data D1 continues until the moment the AND gate 40 is closed.

In response to the rise of the delay clock DCLK, a flip-flop 37 is placed in the set state, thereby opening an AND gate 41 to deliver the image data D2 as the output signal ODP. The output of D2 continues until the delay clock DCLK3 rises.

Thenceforth, and in similar fashion, D3 is outputted as the output signal ODP until DCLK4 rises, and D4 is outputted as the output signal ODP until DCLK1 rises.

Fig. 11 illustrates the operation timing of pulse-width modulation of the input image signal VDO of the second embodiment.

The procedure of image data transmission by the changeover circuit 32 corresponds to carrying out weighting by changing the transmission time with regard to each of the items of image data D1 - D4 by means of the delay clocks DCLK1 - DCLK4.

By adopting the arrangement described above, the maximum operating frequency of the circuit elements of changeover circuit 32 will be about 46.7 MHz if the input frequency of the input image signal VDO is 7 MHz, by way of example. As a result, it will suffice to use elements which operate stably at 50 MHz as the elements of the changeover circuit.

As long as stable operation of the changeover circuit elements is assured, the present invention is not limited as to the number of delay clock signals and the phase differences among them.

In addition, there is no limitation as to the number of bits constituting the input image signal or the number of items of image data inputted to the changeover circuit.

In accordance with this embodiment, as described above, the input image signal can be subjected to pulse-width modulation in a time unit shorter than the period of the master clock signal without altering the master clock period within one period of the input image signals.

Furthermore, a multivalued input recording is converted into a plurality of different signals having lengths of time shorter than the period of the master clock signal without altering the period of the master clock signal within one period of the input image signal, thereby making it possible to perform pulse-width modulation in accordance with a predetermined weighting.

Thus, in accordance with the present invention as described above, there is provided an image signal converting method in which a high-tone recording signal can be obtained without raising the frequency of the master clock signal, and in which a high resolution can be realized economically by using expensive, high-speed operating circuit elements solely within the minimum necessary range.

As many apparently widely different embodiments of the present invention can be made without departing from the scope thereof, it is to be understood that the invention is not limited to the specific embodiments thereof.

Claims

1. A pulse width modulating circuit for modulating a multivalued input signal (VDO) into a pulse signal (OPD) having a corresponding pulse width, the circuit comprising:

converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) for converting the multivalued input signal (VDO) into a plurality of parallel binary signals (D1, D2; D1-D4);
clock generating means (10; 31) for providing a first clock signal (CLK); and
forming means (15; 32) for forming a pulse width modulated signal (OPD) from said plurality of parallel binary signals (D1, D2; D1-D4) using said first clock signal (CLK), said pulse width modulated signal (OPD) having a minimum pulse width shorter than a period of said first clock signal (CLK).

characterised in that:

said converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) is adapted to generate said plurality of binary signals (D1, D2; D1-D4) having equal

pulse widths;
said clock generating means (10; 31) is adapted to generate a plurality of second clock signals (SCLK1, SCLK2; DCLK1-DCLK4) from said first clock signal (CLK), said second clock signals (SCLK1, SCLK2; DCLK1-DCLK4) being of the same frequency but of mutually different phases and corresponding in number to the number of said plurality of parallel binary signals (D1, D2; D1-D4); and
said forming means (15; 32) is adapted to output each of said plurality of parallel binary signals (D1, D2; D1-D4) in phase sequence determined by said second clock signals (SCLK1,SCLK2; DCLK1-DCLK4) to form said pulse width modulated signal (OPD).

2. A pulse width modulating circuit as claimed in claim 1 wherein said forming means (15; 32) includes selecting means (17-19; 36-39, 40-43) for sequentially selecting each of said plurality of parallel binary signals (D1, D2; D1-D4) to combining means (20; 44) to form said pulse width modulated signal (OPD).

3. A pulse width modulating circuit as claimed in claim 1 or claim 2 in which the converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) includes means (1) for splitting the multivalued input signal (VDO) into a plurality of paths.

4. A pulse width modulating circuit as claimed in claim 3, wherein said converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) includes a plurality of comparators (4, 5) each connected to one of said paths, each comparator (4, 5) being adapted to convert the multivalued input signal (VDO) supplied thereto into one of said plurality of parallel binary signals (D1, D2).

5. A pulse width modulating circuit as claimed in claim 4 wherein said comparators (4, 5) are each provided with a respective digital sawtooth waveform (CMPD1, CMPD2) for comparison with the multivalued input signal (VDO) in respective paths.

6. A pulse width modulating circuit as claimed in claim 5 wherein said converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) includes a plurality of latches (2, 3) each connected to one of said paths, each said latch (2, 3) being adapted to receive the multivalued input signal (VDO) and a said second clock signal (SCLK1, SCLK2) and to output the multivalued input signal (VDO) synchronously with the second clock signal (SCLK1, SCLK2) to a respective said comparator (4, 5).

7. A pulse width modulating circuit as claimed in any preceding claim wherein said forming means (15) comprises a flip-flop (17) having said second clock signals (SCLK1, SCLK2) as inputs; a plurality of AND gates (18, 19) each AND gate combining one of said binary signals (D1, D2) and an output of said flip-flop (17); and an OR gate (20) connected to the outputs of said AND gates (18, 19) to form said pulse width modulated signal (OPD).

8. A pulse width modulating circuit as claimed in any preceding claim, wherein said clock generating means (10; 31) includes delay means (10, 31) for delaying said first clock signal (CLK) to generate said second clock signals (SCLK1, SCLK2; DCLK1-DCLK4).

9. A pulse width modulating circuit as claimed in claim 1 wherein said converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) includes a storage table (29) for storing said plurality of parallel binary signals, and an address converting circuit (28) which converts values in the multivalued input signal (VDO) into addresses of said storage table (29) for addressing data in said storage table (29) to output said plurality of parallel binary signals (D1-D4).

10. A pulse width modulating circuit as claimed in claim 9 wherein said storage table (29) is adapted to store said plurality of parallel binary signals where each said binary signal has a different weighting; and said clock generating means (10; 31) is adapted to generate said second clock signals (DCLK1-DCLK4) with mutual phase differences which are weighted accordingly.

11. A pulse width modulating circuit as claimed in claim 10 wherein said forming means (32) comprises a plurality of flip-flops (36-39) connected at inputs thereof to said second clock signals (DCLK1-DCLK4); a plurality of AND gates (40-43), each AND gate (40-43) combining one of said binary signals (D1-D4) and an output of a respective said flip-flop (36-39); and an OR gate (44) connected to the outputs of said AND gates (40-43) to form said pulse width modulated signals (OPD).

12. A pulse width modulated circuit as claimed in claim 1 wherein said converting means (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) is adapted to convert the multivalued input digital signal (VDO) into a plurality of parallel binary signals (D1-D4) having different weightings; and said clock generating means (10; 31) is adapted to generate said second clock signals (DCLK1-DCLK4) with mutual phase differences which are weighted accordingly.

13. Image forming apparatus comprising:

the pulse width modulating circuit as claimed in

any preceding claim for pulse width modulating said multivalued input signal (VDO) comprising pixel data; and
image forming means for receiving said pulse width modulated signal (OPD) and forming an image.

14. Image forming apparatus as claimed in claim 13 wherein said image forming means comprises irradiating means for irradiating a light sensitive body with light modulated by said pulse width modulated signal (OPD).

15. A method of generating a pulse width modulated signal (OPD) from a multivalued input signal (VDO), the method comprising the steps of:

converting the multivalued input signal (VDO) into a plurality of parallel binary signals (D1, D2; D1-D4);
providing a first clock signal (CLK); and
forming a pulse width modulated signal (OPD) from said plurality of parallel binary signals (D1, D2; D1-D4) using said first clock signals (CLK), said pulse width modulated signal (OPD) having a minimum pulse width shorter than a period of said first clock signal (CLK);

characterised in that:

said plurality of binary signals (D1, D2; D1-D4) are generated by the converting step to have equal pulse widths;
a plurality of second clock signals (SCLK1, SCLK2; DCLK1-DCLK4) are generated from said first clock signal (CLK), said second clock signals (SCLK1, SCLK2; DCLK1-DCLK4) being of the same frequency but of mutually different phases and corresponding to the number of said plurality of parallel binary signals (D1, D2; D1-D4); and
outputting each of said plurality of parallel binary signals (D1, D2; D1-D4) in phase sequence determined by said second clock signals (SCLK1, SCLK2; DCLK1-DCLK4) to form said pulse width modulated signal (OPD).

16. Method as claimed in claim 15 wherein the pulse width modulated signal (OPD) is formed by sequentially selecting each of said plurality of parallel binary signals (D1, D2; D1-D4) to be combined to form said pulse width modulated signal (OPD).

17. A method as claimed in claim 15 or claim 16 wherein the multivalued input signal (VDO) is split into a plurality of paths.

18. A method as claimed in claim 17 wherein the multivalued input signal (VDO) in each said plurality of paths is converted into one of said plurality of parallel binary signals (D1, D2) by a respective comparator (4, 5).

19. A method as claimed in claim 18 wherein said comparators (4, 5) are each provided with a respective digital sawtooth waveform (CMPD1, CMPD2) for comparison with the multivalued input signal (VDO) in respective paths.

20. A method as claimed in claim 19 wherein the multivalued input signal (VDO) is input into a latch (2, 3) in each said path, and the multivalued input signal (VDO) is output in response to the said second clock signal (SCLK1, SCLK2) for input to a respective comparator (4, 5).

21. A method as claimed in any one of claims 15 to 20 wherein said second clock signals (SCLK1, SCLK2) are input to a flip-flop (17), an output of the flip-flop (17) and a respective one of said parallel binary signals (D1, D2) are combined by a respective AND gate (18, 19), and the output of the AND gates (18, 19) are input to an OR gate (20) to form said pulse width modulated signal (OPD).

22. A method as claimed in any one of claims 15 to 21 wherein said second clock signals are generated using respective delays.

23. A method as claimed in claim 15 or claim 16 wherein the multivalued input signal (VDO) is converted into addresses of a storage table (29) for addressing data in the storage table (29) to output said plurality of parallel binary signals (D1-D4) which are stored in the storage table (29).

24. A method as claimed in claim 23 wherein said storage table (29) stores said plurality of parallel binary signals which each have a different weighting, and said second clock signals (DCLK1-DCLK4) are generated with mutual phase differences which are weighted accordingly.

25. A method as claimed in claim 24 wherein each said second clock signal (DCLK1-DCLK4) is input to a respective flip-flop (36-39), an output of a respective flip-flop (36-39) and a respective one of said plurality of parallel binary signals (D1-D4) being input to a respective AND gate (40-43), the outputs of the AND gates (40-43) being input into an OR gate (44) to form said pulse width modulated signal (OPD).

26. A method as claimed in claim 15 or claim 16 wherein said multivalued input digital signal (VDO) is converted into a plurality of binary signals having differ-

ent weightings; and said second clock signals (DCLK1-DCLK4) are generated with mutual phase differences which are weighted accordingly.

27. A method of forming an image comprising forming a pulse width modulated signal (OPD) from said multivalued input signal (VDO) comprising pixel data using the method of any one of claims 15 to 26; and forming an image using said pulse width modulated signal (OPD).

28. A method as claimed in claim 27 wherein step of forming an image comprises the step of irradiating a light sensitive body with light modulated by said pulse width modulated signal (OPD).

Patentansprüche

1. Pulsbreitenmodulationsschaltung zur Modulation eines mehrwertigen Eingangssignals (VDO) in ein Impulssignal (OPD) mit einer entsprechenden Impulsbreite mit

einer Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) zur Umwandlung des mehrwertigen Eingangssignals (VDO) in eine Vielzahl von parallelen Binärsignalen (D1, D2; D1-D4),
einer Takterzeugungseinrichtung (10; 31) zur Bereitstellung eines ersten Taktsignals (CLK) und
einer Ausbildungseinrichtung (15; 32) zur Ausbildung eines pulsbreitenmodulierten Signals (OPD) aus der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) unter Verwendung des ersten Taktsignals (CLK), wobei das pulsbreitenmodulierte Signal (OPD) eine minimale Impulsbreite aufweist, die kleiner als eine Periode des ersten Taktsignals (CLK) ist,

dadurch gekennzeichnet, daß

die Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) zur Erzeugung der Vielzahl der Binärsignale (D1, D2; D1-D4) mit gleichen Impulsbreiten angepaßt ist,
die Takterzeugungseinrichtung (10; 31) zur Erzeugung einer Vielzahl von zweiten Taktsignalen (SCLK1, SCLK2; DCLK1-DCLK4) aus dem ersten Taktsignal (CLK) angepaßt ist, wobei die zweiten Taktsignale (SCLK1, SCLK2; DCLK1-DCLK4) die gleiche Frequenz aber gegenseitig verschiedene Phasen aufweisen und in der Anzahl der Anzahl der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) entsprechen, und
die Ausbildungseinrichtung (15; 32) zur Ausgabe jedes der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) in einer durch die zweiten Taktsignale (SCLK1, SCLK2; DCLK1-DCLK4) bestimmten Phasenfolge angepaßt ist, um das pulsbreitenmodulierte Signal (OPD) auszubilden.

2. Pulsbreitenmodulationsschaltung nach Anspruch 1,
dadurch gekennzeichnet, daß
die Ausbildungseinrichtung (15; 32) eine Auswahleinrichtung (17-19; 36-39, 40-43) zur aufeinanderfolgenden Auswahl jedes der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) für eine Verbindungseinrichtung (20; 44) zur Ausbildung des pulsbreitenmodulierten Signals (OPD) enthält.

3. Pulsbreitenmodulationsschaltung nach Anspruch 1 oder 2,
dadurch gekennzeichnet, daß
die Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) eine Einrichtung (1) zum Aufspalten des mehrwertigen Eingangssignals (VDO) in eine Vielzahl von Pfaden enthält.

4. Pulsbreitenmodulationsschaltung nach Anspruch 3,
dadurch gekennzeichnet, daß
Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) eine Vielzahl von Vergleichereinrichtungen (4, 5) enthält, die jeweils mit einem der Pfade verbunden sind, wobei jede Vergleichereinrichtung (4, 5) zur Umwandlung des zugeführten mehrwertigen Eingangssignals (VDO) in eines der Vielzahl der parallelen Binärsignale (D1, D2) angepaßt ist.

5. Pulsbreitenmodulationsschaltung nach Anspruch 4,
dadurch gekennzeichnet, daß
die Vergleichereinrichtungen (4, 5) jeweils mit einem jeweiligen digitalen Sägezahnsignalverlauf (CMPD1, CMPD2) zum Vergleich mit dem mehrwertigen Eingangssignal (VDO) auf jeweiligen Pfaden versehen sind.

6. Pulsbreitenmodulationsschaltung nach Anspruch 5,
dadurch gekennzeichnet, daß
die Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) eine Vielzahl von Signalspeichern (2, 3) enthält, die jeweils mit einem der Pfade verbunden sind, wobei jeder Signalspeicher (2, 3) zum Empfang des mehrwertigen Eingangssignals (VDO) und des zweiten Taktsignals (SCLK1, SCLK2) und zur Ausgabe des mehrwertigen Eingangssignals (VDO) synchron mit dem zweiten Taktsignal (SCLK1, SCLK2) an die jeweilige Vergleichereinrichtung (4, 5) angepaßt ist.

7. Pulsbreitenmodulationsschaltung nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, daß
die Ausbildungseinrichtung (15) ein Flip-Flop (17) mit den zweiten Taktsignalen (SCLK1, SCLK2) als Eingangssignale, eine Vielzahl von UND-Gattern (18, 19), wobei jedes UND-Gatter eines der Binärsignale (D1, D2) und ein Ausgangssignal des Flip-Flops (17) verbindet, und ein ODER-Gatter (20) enthält, das mit den Ausgängen der UND-Gatter (18, 19) zur Ausbildung des pulsbreitenmodulierten Signals (OPD) verbunden ist.

8. Pulsbreitenmodulationsschaltung nach einem der vorhergehenden Ansprüche,
dadurch gekennzeichnet, daß
die Takterzeugungseinrichtung (10; 31) eine Verzögerungseinrichtung (10, 31) zur Verzögerung des ersten Taktsignals (CLK) zur Erzeugung der zweiten Taktsignale (SCLK1, SCLK2; DCLK1-DCLK4) enthält.

9. Pulsbreitenmodulationsschaltung nach Anspruch 1,
dadurch gekennzeichnet, daß
die Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) eine Speichertabelle (29) zur Speicherung der Vielzahl der parallelen Binärsignale und eine Adressenumwandlungsschaltung (28) enthält, die Werte in demmehrwertigen Eingangssignal (VDO) in Adressen der Speichertabelle (29) zur Adressierung von Daten in der Speichertabelle (29) zur Ausgabe der Vielzahl der parallelen Binärsignale (D1-D4) umwandelt.

10. Pulsbreitenmodulationsschaltung nach Anspruch 9,
dadurch gekennzeichnet, daß
die Speichertabelle (29) zur Speicherung der Vielzahl der parallelen Binärsignale angepaßt ist, wobei jedes der Binärsignale eine unterschiedliche Gewichtung aufweist, und die Takterzeugungseinrichtung (10; 31) zur Erzeugung der zweiten Taktsignale (DCLK1-DCLK4) mit gegenseitigen Phasendifferenzen angepaßt ist, die entsprechend gewichtet sind.

11. Pulsbreitenmodulationsschaltung nach Anspruch 10,
dadurch gekennzeichnet, daß
die Ausbildungseinrichtung (32) eine Vielzahl von Flip-Flops (36-39), deren Eingänge mit den zweiten Taktsignalen (DCLK1-DCLK4) verbunden sind, eine Vielzahl von UND-Gattern (40-43), wobei jedes UND-Gatter (40-43) eines der Binärsignale (D1-D4) und ein Ausgangssignal des jeweiligen Flip-Flops (36-39) verbindet, und ein ODER-Gatter (44) aufweist, das mit den Ausgängen der UND-Gatter (40-43) zur Ausbildung des pulsbreitenmodulierten Signals (OPD) verbunden ist.

12. Pulsbreitenmodulationsschaltung nach Anspruch 1,
dadurch gekennzeichnet, daß
die Umwandlungseinrichtung (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) zur Umwandlung des mehrwertigen digitalen Eingangssignals (VDO) in eine Vielzahl von parallelen Binärsignalen (D1-D4) mit unterschiedlichen Gewichtungen angepaßt ist und die Takterzeugungseinrichtung (10; 31) zur Erzeugung der zweiten Taktsignale (DCLK1-DCLK4) mit gegenseitigen Phasendifferenzen angepaßt ist, die entsprechend gewichtet sind.

13. Bildausbildungsvorrichtung mit

der Pulsbreitenmodulationsschaltung nach einem der vorhergehenden Ansprüche zur Pulsbreitenmodulation des Bildelementdaten aufweisenden mehrwertigen Eingangssignals (VDO) und
einer Bildausbildungseinrichtung zum Empfang des pulsbreitenmodulierten Signals (OPD) und zur Ausbildung eines Bildes.

14. Bildausbildungsvorrichtung nach Anspruch 13, wobei die Bildausbildungseinrichtung eine Bestrahlungseinrichtung zur Bestrahlung eines lichtempfindlichen Körpers mit durch das pulsbreitenmodulierte Signal (OPD) moduliertem Licht.

15. Verfahren zur Erzeugung eines pulsbreitenmodulierten Signals (OPD) aus einem mehrwertigen Eingangssignal (VDO) mit den Schritten

Umwandeln des mehrwertigen Eingangssignals (VDO) in eine Vielzahl von parallelen Binärsignalen (D1, D2; D1-D4),
Bereitstellen eines ersten Taktsignals (CLK) und
Ausbilden eines pulsbreitenmodulierten Signals (OPD) aus der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) unter Verwendung des ersten Taktsignals (CLK), wobei das pulsbreitenmodulierte Signal (OPD) eine minimale Impulsbreite aufweist, die kleiner als eine Periode des ersten Taktsignals (CLK) ist,

dadurch gekennzeichnet, daß

die Vielzahl der Binärsignale (D1, D2; D1-D4) durch den Umwandlungsschritt derart erzeugt werden, daß sie gleiche Impulsbreiten aufweisen,
eine Vielzahl von zweiten Taktsignalen (SCLK1, SCLK2; DCLK1-DCLK4) aus dem er-

sten Taktsignal (CLK) erzeugt werden, wobei die zweiten Taktsignale (SCLK1, SCLK2; DCLK1-DCLK4) die gleiche Frequenz aber gegenseitig verschiedene Phasen aufweisen und der Anzahl der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) entsprechen, und jedes der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) in einer durch die zweiten Taktsignale (SCLK1, SCLK2; DCLK1-DCLK4) bestimmten Phasenfolge zur Ausbildung des pulsbreitenmodulierten Signals (OPD) ausgegeben wird.

16. Verfahren nach Anspruch 15,
dadurch gekennzeichnet, daß
das pulsbreitenmodulierte Signal (OPD) durch aufeinanderfolgende Auswahl jedes der Vielzahl der parallelen Binärsignale (D1, D2; D1-D4) ausgebildet wird, die zur Ausbildung des pulsbreitenmodulierten Signals (OPD) zu verbinden sind.

17. Verfahren nach Anspruch 15 oder 16,
dadurch gekennzeichnet, daß
das mehrwertige Eingangssignal (VDO) in eine Vielzahl von Pfaden aufgespalten wird.

18. Verfahren nach Anspruch 17,
dadurch gekennzeichnet, daß
das mehrwertige Eingangssignal (VDO) auf jedem der Vielzahl der Pfade durch eine jeweilige Vergleichereinrichtung (4, 5) in eines der Vielzahl der parallelen Binärsignale (D1, D2) umgewandelt wird.

19. Verfahren nach Anspruch 18,
dadurch gekennzeichnet, daß
die Vergleichereinrichtungen (4, 5) jeweils mit einem jeweiligen digitalen Sägezahnsignalverlauf (CMPD1, CMPD2) zum Vergleich mit dem mehrwertigen Eingangssignal (VDO) auf jeweiligen Pfaden versehen sind.

20. Verfahren nach Anspruch 19,
dadurch gekennzeichnet, daß
das mehrwertige Eingangssignal (VDO) in einen Signalspeicher (2, 3) auf jedem Pfad eingegeben wird und das mehrwertige Eingangssignals (VDO) beruhend auf dem zweiten Taktsignal (SCLK1, SCLK2) zur Eingabe in eine jeweilige Vergleichereinrichtung (4, 5) ausgegeben wird.

21. Verfahren nach einem der Ansprüche 15 bis 20,
dadurch gekennzeichnet, daß
die zweiten Taktsignale (SCLK1, SCLK2) in ein Flip-Flop (17) eingegeben werden, ein Ausgangssignal des Flip-Flops (17) und ein jeweiliges der parallelen Binärsignale (D1, D2) durch ein jeweiliges UND-Gatter (18, 19) verbunden werden und die Ausgangssignale der UND-Gatter (18, 19) in ein ODER-Gatter (20) zur Ausbildung des pulsbreitenmodulierten Signals (OPD) eingegeben werden.

22. Verfahren nach einem der Ansprüche 15 bis 21,
dadurch gekennzeichnet, daß
die zweiten Taktsignale unter Verwendung jeweiliger Verzögerungen erzeugt werden.

23. Verfahren nach Anspruch 15 oder 16,
dadurch gekennzeichnet, daß
das mehrwertige Eingangssignal (VDO) in Adressen einer Speichertabelle (29) zur Adressierung von Daten in der Speichertabelle (29) zur Ausgabe der Vielzahl der parallelen Binärsignale (D1-D4) umgewandelt wird, die in der Speichertabelle (29) gespeichert sind.

24. Verfahren nach Anspruch 23,
dadurch gekennzeichnet, daß
die Speichertabelle (29) die Vielzahl der parallelen Binärsignale speichert, die jeweils eine unterschiedliche Gewichtung aufweisen, und die zweiten Taktsignale (DCLK1-DCLK4) mit gegenseitigen Phasendifferenzen erzeugt werden, die entsprechend gewichtet sind.

25. Verfahren nach Anspruch 24,
dadurch gekennzeichnet, daß
jedes zweite Taktsignal (DCLK1-DCLK4) in ein jeweiliges Flip-Flop (36-39) eingegeben wird, wobei ein Ausgangssignal eines jeweiligen Flip-Flops (36-39) und ein jeweiliges der Vielzahl der parallelen Binärsignale (D1-D4) in ein jeweiliges UND-Gatter (40-43) eingegeben werden, und wobei die Ausgangssignale der UND-Gatter (40-43) in ein ODER-Gatter (44) zur Ausbildung des pulsbreitenmodulierten Signals (OPD) eingegeben werden.

26. Verfahren nach Anspruch 15 oder 16,
dadurch gekennzeichnet, daß
das mehrwertige digitale Eingangssignal (VDO) in eine Vielzahl von Binärsignalen mit unterschiedlichen Gewichtungen umgewandelt wird und die zweiten Taktsignale (DCLK1-DCLK4) mit gegenseitigen Phasendifferenzen erzeugt werden, die entsprechend gewichtet sind.

27. Verfahren zur Ausbildung eines Bildes mit den Schritten

Ausbilden eines pulsbreitenmodulierten Signals (OPD) aus dem Bildelementdaten aufweisenden mehrwertigen Eingangssignal (VDO) unter Verwendung des Verfahrens nach einem der Ansprüche 15 bis 26 und
Ausbilden eines Bildes unter Verwendung des pulsbreitenmodulierten Signals (OPD).

28. Verfahren nach Anspruch 27, wobei der Schritt zur Ausbildung eines Bildes den Schritt zur Bestrahlung eines lichtempfindlichen Körpers mit durch das pulsbreitenmodulierte Signal (OPD) moduliertem Licht aufweist.

Revendications

1. Circuit de modulation en largeur d'impulsion pour moduler un signal d'entrée (VDO) à valeurs multiples en un signal (OPD) d'impulsion ayant une largeur d'impulsion correspondante, le circuit comprenant:

un moyen (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) de conversion pour convertir le signal (VDO) d'entrée à valeurs multiples en une pluralité de signaux (D1, D2; D1-D4) binaires parallèles;
un moyen (10; 31) de génération d'horloge pour fournir un premier signal (CLK) d'horloge; et
un moyen (15; 32) de formation pour former un signal (OPD) modulé en largeur d'impulsion à partir de ladite pluralité de signaux (D1, D2; D1-D4) binaires parallèles en utilisant ledit premier signal (CLK) d'horloge, ledit signal (OPD) modulé en largeur d'impulsion ayant une largeur d'impulsion minimum plus courte que la période dudit premier signal (CLK) d'horloge,

caractérisé en ce que:

ledit moyen (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) de conversion est apte à générer ladite pluralité de signaux binaires (D1, D2; D1-D4) ayant des largeurs d'impulsion égales;
ledit moyen (10; 31) de génération d'horloge est apte à générer une pluralité de seconds signaux (SCLK1, SCLK2; DCLK1-DCLK4) d'horloge à partir dudit premier signal (CLK) d'horloge, lesdits seconds signaux (SCLK1, SCLK2; DCLK1-DCLK4) d'horloge étant de même fréquence mais de phases mutuellement différentes et correspondant en nombre au nombre de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4); et
ledit moyen (15; 32) de formation est apte à délivrer chacun de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4) dans l'ordre des phases déterminé par lesdits seconds signaux (SCLK1, SCLK2; DCLK1-DCLK4) d'horloge pour former ledit signal (OPD) modulé en largeur d'impulsion.

2. Circuit de modulation de largeur d'impulsion selon la revendication 1, dans lequel ledit moyen de formation (15; 32) comporte un moyen de sélection (17-19; 36-39; 40-43) pour sélectionner séquentiellement chacun de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4) pour un moyen de combinaison (20; 44), afin de former ledit signal (OPD) modulé en largeur d'impulsion.

3. Circuit de modulation de largeur d'impulsion selon la revendication 1 ou la revendication 2, dans lequel le moyen de conversion (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) comporte un moyen (1) pour séparer le signal (VDO) d'entrée à valeurs multiples en une pluralité de trajets.

4. Circuit de modulation de largeur d'impulsion selon la revendication 3, dans lequel ledit moyen de conversion (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) comporte une pluralité de comparateurs (4, 5) connectés chacun à l'un desdits trajets, chaque comparateur (4, 5) étant apte à convertir le signal (VDO) d'entrée à valeurs multiples qui lui est appliqué en l'un de ladite pluralité de signaux binaires parallèles (D1, D2).

5. Circuit de modulation de largeur d'impulsion selon la revendication 4, dans lequel lesdits comparateurs (4, 5) sont pourvus chacun d'une forme d'onde en dents de scie numérique respective (CMPD1, CMPD2) pour la comparaison avec le signal (VDO) d'entrée à valeurs multiples, dans des trajets respectifs.

6. Circuit de modulation de largeur d'impulsion selon la revendication 5, dans lequel ledit moyen de conversion (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) comporte une pluralité de dispositifs de verrouillage (2, 3) connectés chacun à l'un desdits trajets, chacun desdits dispositifs de verrouillage (2, 3) étant apte à recevoir le signal (VDO) d'entrée à valeurs multiples et l'un desdits seconds signaux d'horloge (SCLK1, SCLK2) et à délivrer le signal (VDO) d'entrée à valeurs multiples de manière synchrone avec le second signal d'horloge (SCLK1, SCLK2), à un comparateur respectif (4, 5).

7. Circuit de modulation de largeur d'impulsion selon l'une quelconque des revendications précédentes, dans lequel ledit moyen de formation (15) comprend une bascule (17) ayant, en entrées, lesdits seconds signaux d'horloge (SCLK1, SCLK2); une pluralité de portes ET (18, 19), chaque porte ET combinant l'un desdits signaux binaires (D1, D2) et une sortie de ladite bascule (17); et une porte OU (20) connectée aux sorties desdites portes ET (18, 19) pour former ledit signal (OPD) modulé en largeur d'impulsion.

8. Circuit de modulation de largeur d'impulsion selon l'une quelconque des revendications précédentes, dans lequel ledit moyen (10; 31) de génération

d'horloge comporte un moyen à retard (10, 31) pour retarder ledit premier signal d'horloge (CLK) afin de générer lesdits seconds signaux d'horloge (SCLK1, SCLK2; DCLK1-DCLK4).

9. Circuit de modulation de largeur d'impulsion selon la revendication 1, dans lequel ledit moyen de conversion (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) comporte une table (29) de stockage pour stocker ladite pluralité de signaux binaires parallèles, et un circuit (28) de conversion d'adresse qui convertit des valeurs, dans le signal (VDO) d'entrée à valeurs multiples, en adresses de ladite table (29) de stockage pour adresser des données dans ladite table (29) de stockage en vue de délivrer ladite pluralité de signaux binaires parallèles (D1-D4).

10. Circuit de modulation de largeur d'impulsion selon la revendication 9, dans lequel ladite table (29) de stockage est apte à stocker ladite pluralité de signaux binaires parallèles, chacun desdits signaux binaires ayant un poids différent; et ledit moyen (10; 31) de génération d'horloge est apte à générer lesdits seconds signaux d'horloge (DCLK1-DCLK4) avec des différences de phase mutuelles qui sont pondérées en conséquence.

11. Circuit de modulation de largeur d'impulsion selon la revendication 10, dans lequel ledit moyen de formation (32) comprend une pluralité de bascules (36-39) connectées à ses entrées auxdits seconds signaux d'horloge (DCLK1-DCLK4); une pluralité de portes ET (40-43), chaque porte ET (40-43) combinant l'un desdits signaux binaires (D1-D4) et une sortie d'une bascule respective desdites bascules (36-39); et une porte OU (44) connectée aux sorties desdites portes ET (40-43) pour former lesdits signaux (OPD) modulés en largeur d'impulsion.

12. Circuit de modulation en largeur d'impulsion selon la revendication 1, dans lequel ledit moyen de conversion (1, 2, 3, 4, 5, 13, 14; 27, 28, 29, 30) est apte à convertir le signal (VDO) d'entrée à valeurs multiples en une pluralité de signaux binaires parallèles (D1-D4) ayant des poids différents; et ledit moyen (10; 31) de génération d'horloge est apte à générer lesdits seconds signaux d'horloge (DCLK1-DCLK4) avec des différences de phase mutuelles qui sont pondérées en conséquence.

13. Appareil de formation d'image comprenant:

le circuit de modulation de largeur d'impulsion selon l'une quelconque des revendications précédentes, pour moduler en largeur d'impulsion ledit signal (VDO) d'entrée à valeurs multiples comprenant des données de pixel; et
un moyen de formation d'image pour recevoir ledit signal (OPD) modulé en largeur d'impulsion et former une image.

14. Appareil de formation d'image selon la revendication 13, dans lequel ledit moyen de formation d'image comprend un moyen d'irradiation pour irradier un corps sensible à la lumière avec de la lumière modulée par ledit signal (OPD) modulé en largeur d'impulsion.

15. Procédé de génération d'un signal (OPD) modulé en largeur d'impulsion à partir d'un signal (VDO) d'entrée à valeurs multiples, le procédé comprenant les étapes suivantes:

conversion du signal (VDO) d'entrée à valeurs multiples en une pluralité de signaux binaires parallèles (D1, D2; D1-D4);
fourniture d'un premier signal d'horloge (CLK); et
formation d'un signal (OPD) modulé en largeur d'impulsion à partir de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4) en utilisant lesdits premiers signaux d'horloge (CLK), ledit signal (OPD) modulé en largeur d'impulsion ayant une largeur d'impulsion minimum plus courte que la période dudit premier signal d'horloge (CLK);

caractérisé en ce que:

ladite pluralité de signaux binaires (D1, D2; D1-D4) sont générés par l'étape de conversion pour avoir des largeurs d'impulsion égales;
une pluralité de seconds signaux d'horloge (SCLK1, SCLK2; DCLK1-DCLK4) sont générés à partir dudit premier signal d'horloge (CLK), lesdits seconds signaux d'horloge (SCLK1, SCLK2; DCLK1-DCLK4) étant de même fréquence mais de phases mutuellement différentes et correspondant au nombre de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4); et
chacun de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4) est délivré dans l'ordre des phases déterminé par lesdits seconds signaux d'horloge (SCLK1, SCLK2; DCLK1-DCLK4) pour former ledit signal (OPD) modulé en largeur d'impulsion.

16. Procédé selon la revendication 15, dans lequel le signal (OPD) modulé en largeur d'impulsion est formé par sélection séquentielle de chacun de ladite pluralité de signaux binaires parallèles (D1, D2; D1-D4) destinés à être combinés pour former ledit signal (OPD) modulé en largeur d'impulsion.

17. Procédé selon la revendication 15 ou la revendica-

tion 16, dans lequel le signal (VDO) d'entrée à valeurs multiples est séparé en une pluralité de trajets.

18. Procédé selon la revendication 17, dans lequel le signal (VDO) d'entrée à valeurs multiples, dans chacun de ladite pluralité de trajets, est converti en l'un de ladite pluralité de signaux binaires parallèles (D1, D2) par un comparateur respectif (4, 5).

19. Procédé selon la revendication 18, dans lequel lesdits comparateurs (4, 5) sont chacun pourvus d'une forme d'onde en dents de scie numérique respective (CMPD1, CMPD2) pour la comparaison avec le signal (VDO) d'entrée à valeurs multiples, dans des trajets respectifs.

20. Procédé selon la revendication 19, dans lequel le signal (VDO) d'entrée à valeurs multiples est introduit dans un dispositif de verrouillage (2, 3) dans chacun desdits trajets, et le signal (VDO) d'entrée à valeurs multiples est délivré en réponse audit second signal d'horloge (SCLK1, SCLK2) pour l'introduction dans un comparateur respectif (4, 5).

21. Procédé selon l'une quelconque des revendications 15 à 20, dans lequel lesdits seconds signaux d'horloge (SCLK1, SCLK2) sont introduits dans une bascule (17), une sortie de la bascule (17) et un signal respectif desdits signaux binaires parallèles (D1, D2) sont combinés par une porte ET respective (18, 19), et les sorties des portes ET (18, 19) sont introduites dans une porte OU (20) pour former ledit signal (OPD) modulé en largeur d'impulsion.

22. Procédé selon l'une quelconque des revendications 15 à 21, dans lequel lesdits seconds signaux d'horloge sont générés en utilisant des retards respectifs.

23. Procédé selon la revendication 15 ou la revendication 16, dans lequel le signal (VDO) d'entrée à valeurs multiples est converti en adresses d'une table (29) de stockage pour adresser des données dans la table (29) de stockage en vue de délivrer ladite pluralité de signaux binaires parallèles (D1-D4) qui sont stockés dans la table (29) de stockage.

24. Procédé selon la revendication 23, dans lequel ladite table (29) de stockage stocke ladite pluralité de signaux binaires parallèles qui ont chacun un poids différent, et lesdits seconds signaux d'horloge (DCLK1-DCLK4) sont générés avec des différences de phase mutuelles qui sont pondérées en conséquence.

25. Procédé selon la revendication 24, dans lequel chacun desdits seconds signaux d'horloge (DCLK1-DCLK4) est introduit dans une bascule respective (36-39), une sortie d'une bascule respective (36-39) et un signal respectif de ladite pluralité de signaux binaires parallèles (D1-D4) étant introduits dans une porte ET respective (40-43), les sorties des portes ET (40-43) étant introduites dans une porte OU (44) pour former ledit signal (OPD) modulé en largeur d'impulsion.

26. Procédé selon la revendication 15 ou la revendication 16, dans lequel ledit signal (VDO) numérique d'entrée à valeurs multiples est converti en une pluralité de signaux binaires ayant des poids différents; et lesdits seconds signaux d'horloge (DCLK1-DCLK4) sont générés avec des différences de phase mutuelles qui sont pondérées en conséquence.

27. Procédé de formation d'une image comprenant la formation d'un signal (OPD) modulé en largeur d'impulsion à partir dudit signal (VDO) d'entrée à valeurs multiples comprenant des données de pixel en utilisant le procédé selon l'une quelconque des revendications 15 à 26; et de formation d'une image en utilisant ledit signal (OPD) modulé en largeur d'impulsion.

28. Procédé selon la revendication 27, dans lequel l'étape de formation d'une image comprend l'étape d'irradiation d'un corps sensible à la lumière avec de la lumière modulée par ledit signal (OPD) modulé en largeur d'impulsion.

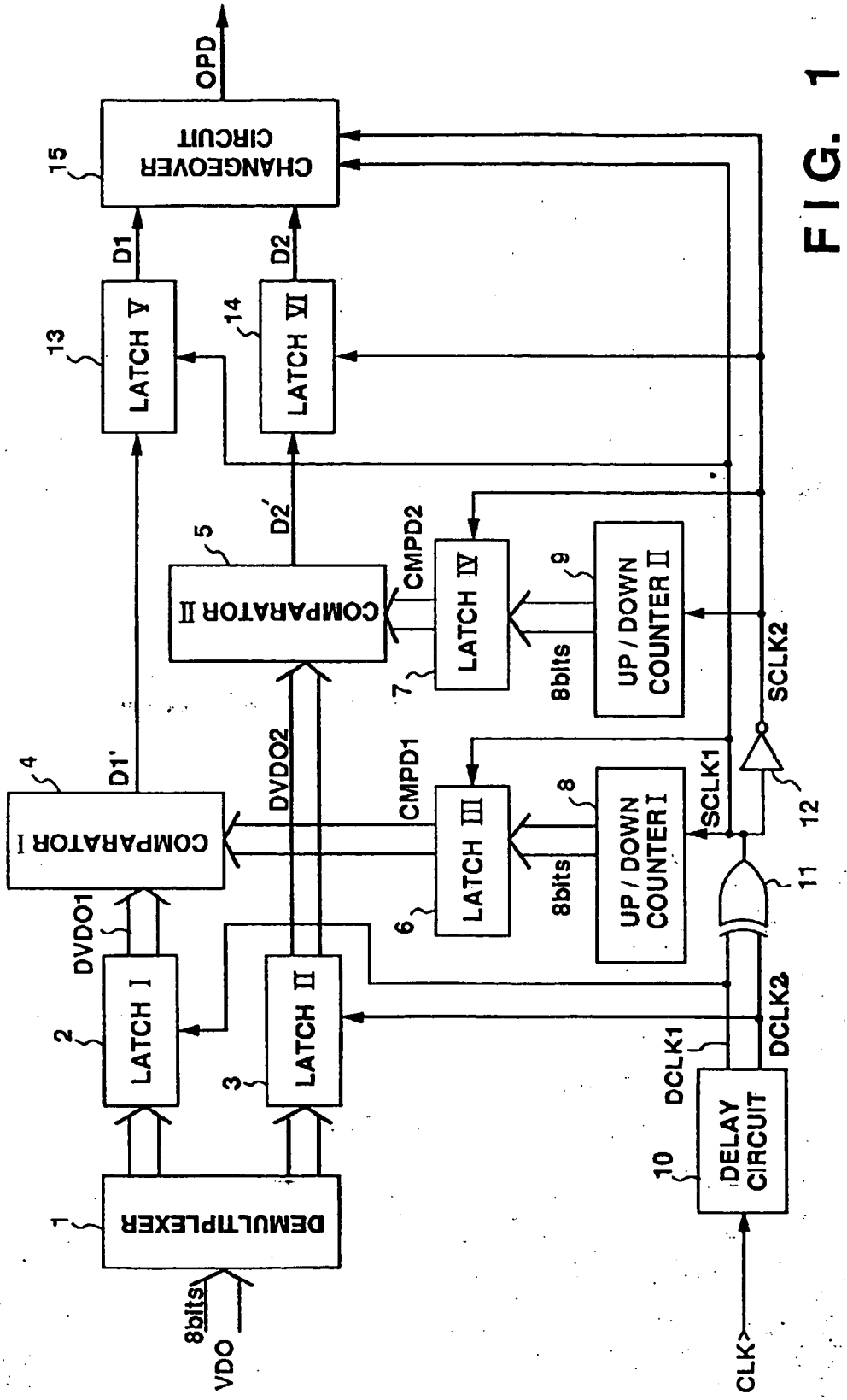
OPD
CHANGEOVER CIRCUIT
15
D1
D2
LATCH V
LATCH VI
13
14
D2'
5
COMPARATOR II
CMPD2
LATCH IV
9
UP / DOWN COUNTER II
7
8bits
SCLK2
4
D1'
COMPARATOR I
DVDO2
CMPD1
LATCH III
8
UP / DOWN COUNTER I
SCLK1
12
11
DVDO1
6
8bits
LATCH I
LATCH II
2
3
DCLK2
DCLK1
DELAY CIRCUIT
10
DEMULTIPLEXER
1
8bits
VDO
CLK

FIG. 1

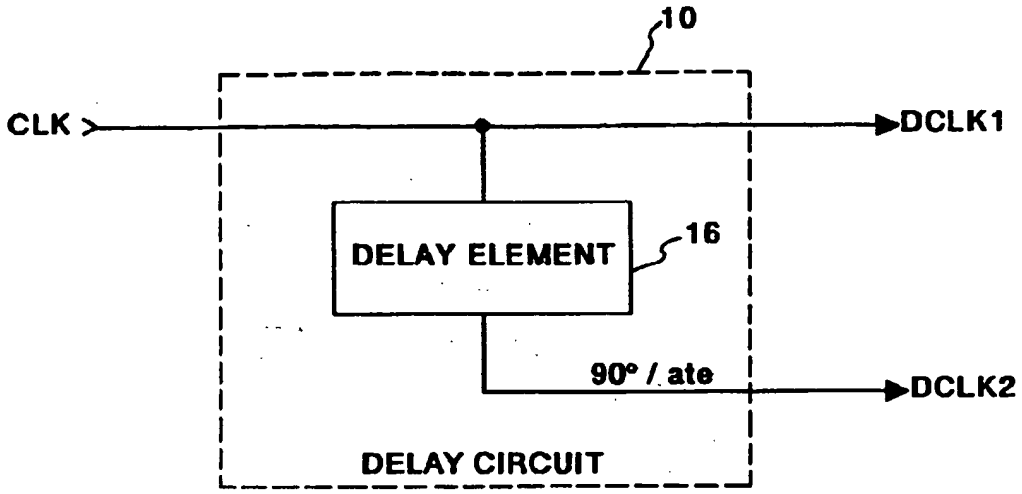
10
CLK
DCLK1
DELAY ELEMENT
16
90° / ate
DCLK2
DELAY CIRCUIT

FIG. 2

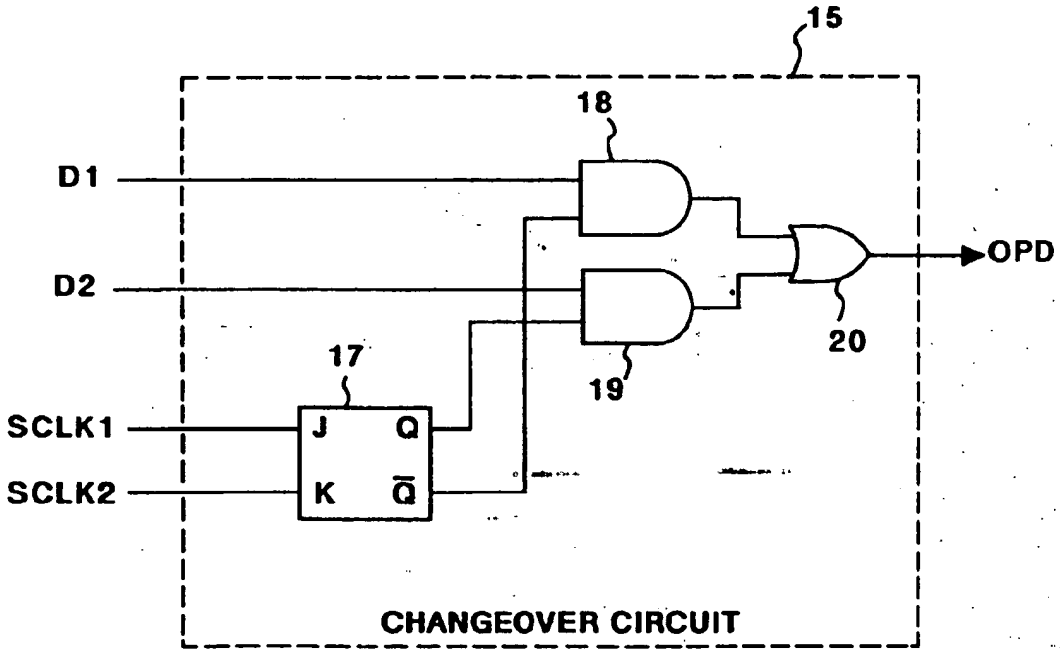
15
18
D1
D2
OPD
20
17
19
SCLK1
SCLK2
J
Q
K
Q̄
CHANGEOVER CIRCUIT

FIG. 3

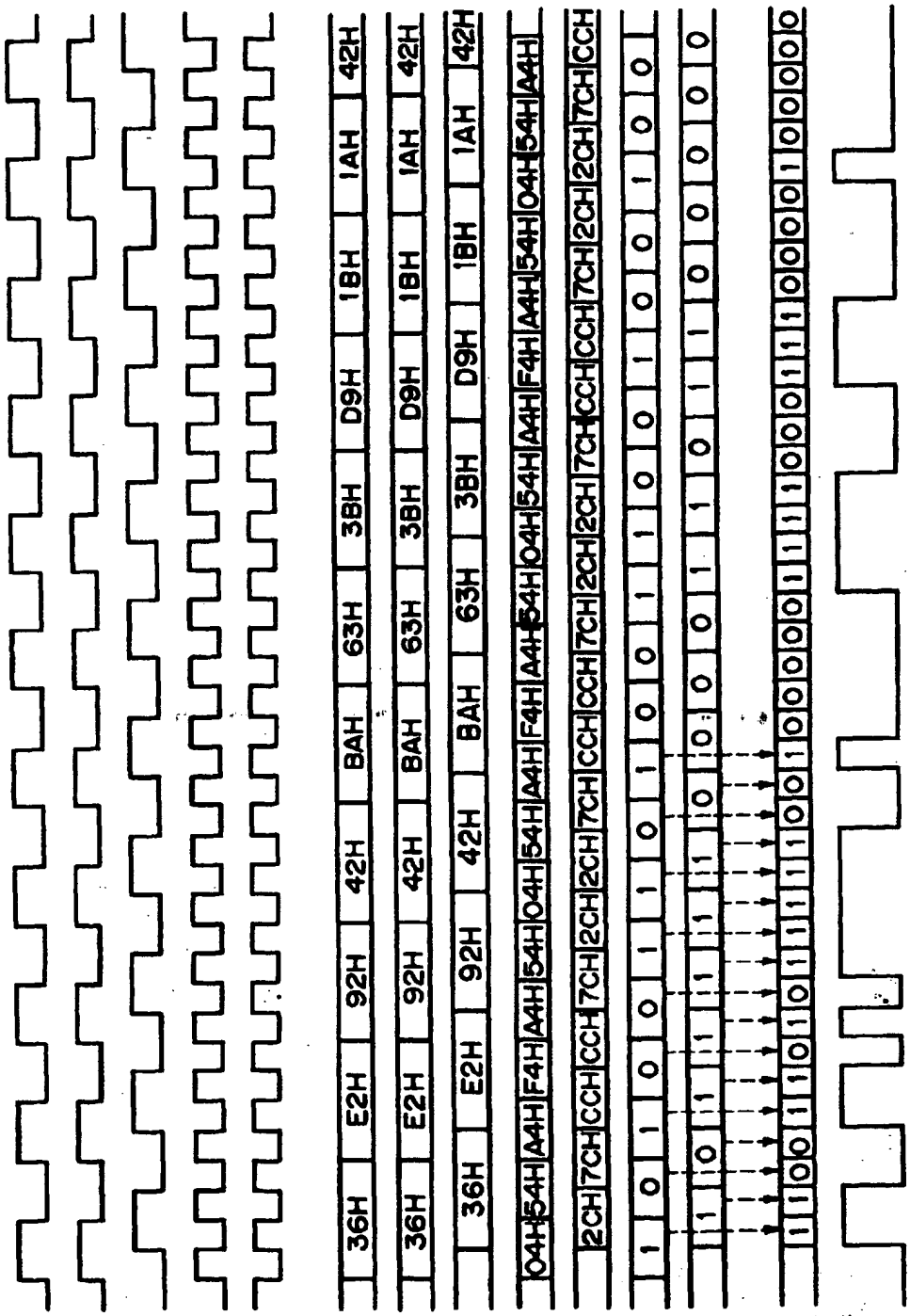
CLK
DCLK1
DCLK2
SCLK1
SCLK2
VDO
DVDO1
DVDO2
CMPD1
CMPD2
D1
D2
OPD
36H E2H 92H 42H BAH 63H 3BH D9H 1BH 1AH 42H
36H E2H 92H 42H BAH 63H 3BH D9H 1BH 1AH 42H
36H E2H 92H 42H BAH 63H 3BH D9H 1BH 1AH 42H
04H 54H A4H F4H A4H 54H 04H 54H A4H F4H A4H 54H 04H 54H A4H
2CH 7CH CCH CCH 7CH 2CH 2CH 7CH CCH CCH 7CH 2CH 2CH 7CH CCH

FIG. 4

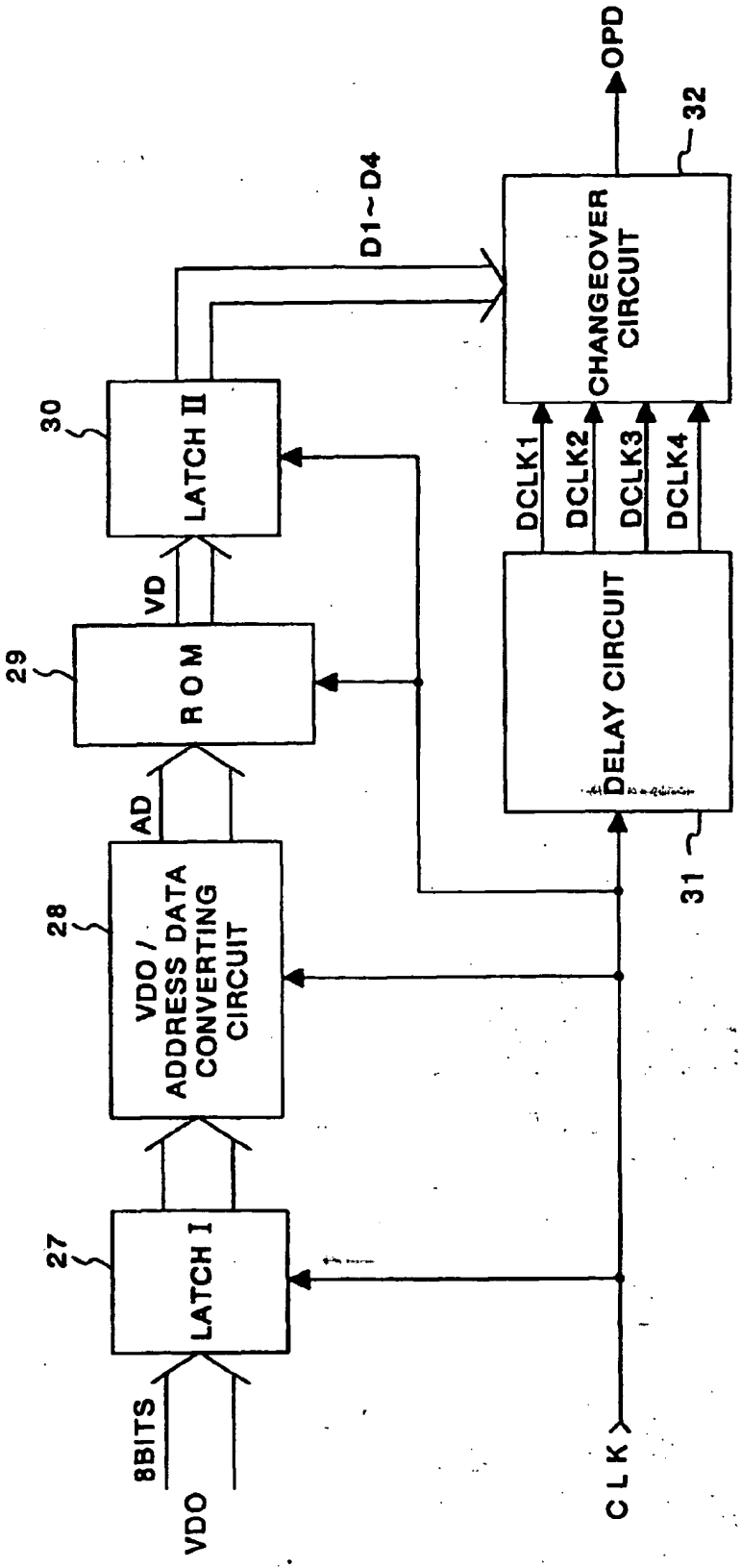
VDO
8BITS
LATCH I
27
VDO / ADDRESS DATA CONVERTING CIRCUIT
28
AD
ROM
29
VD
LATCH II
30
D1~D4
CHANGEOVER CIRCUIT
32
OPD
DCLK1
DCLK2
DCLK3
DCLK4
DELAY CIRCUIT
31
CLK

FIG. 5

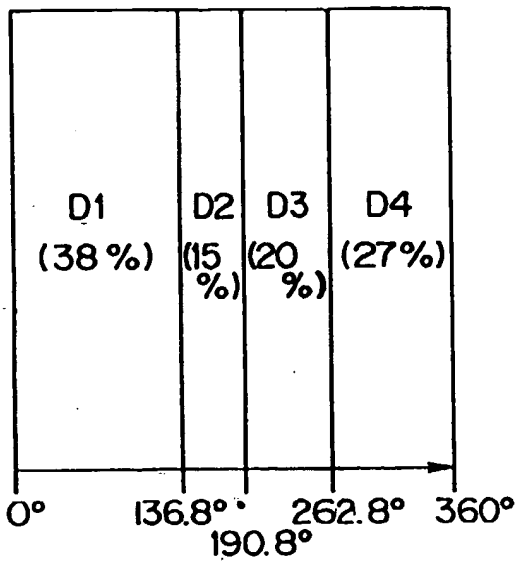
D1
(38 %)
D2
(15 %)
D3
(20 %)
D4
(27%)
0°
136.8°
190.8°
262.8°
360°

FIG. 6

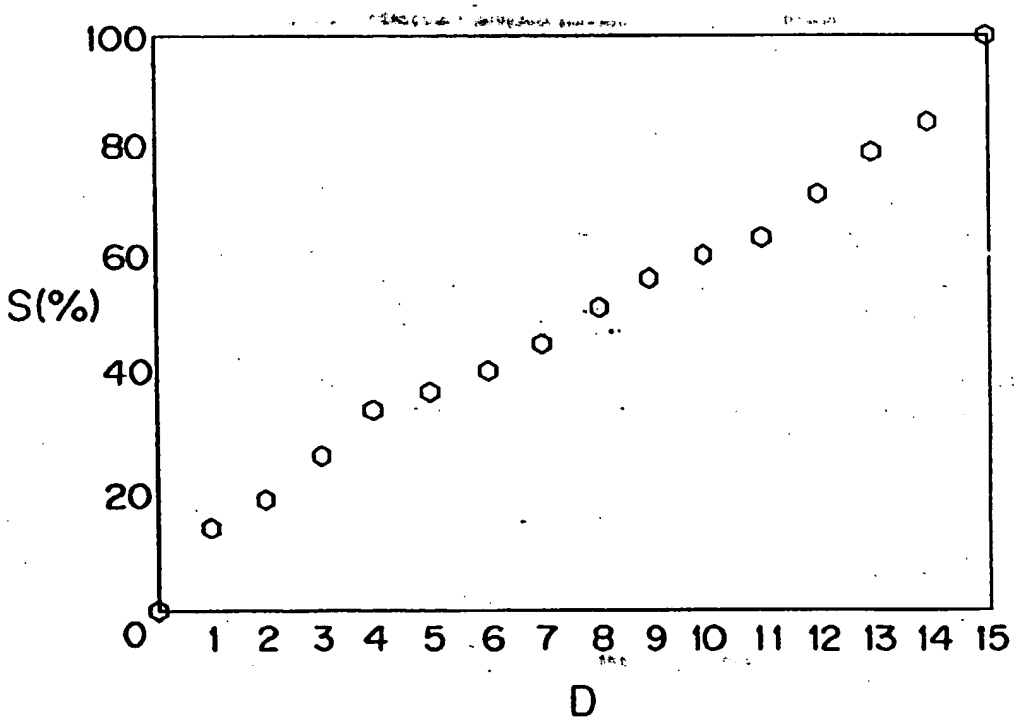
100
80
60
40
20
0
S(%)
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
D

FIG. 7

D	S (%)	VDO	VD			
			D1	D2	D3	D4
0	0	00H ~ 13H	0	0	0	0
1	15	14H ~ 2CH	0	1	0	0
2	20	2DH ~ 3CH	0	0	1	0
3	27	3DH ~ 4FH	0	0	0	1
4	35	50H ~ 5DH	0	1	1	0
5	38	5EH ~ 66H	1	0	0	0
6	42	67H ~ 71H	0	1	0	1
7	47	72H ~ 7FH	0	0	1	1
8	53	80H ~ 8DH	1	1	0	0
9	58	8EH ~ 99H	1	0	1	0
10	62	9AH ~ A2H	0	1	1	1
11	65	A3H ~ B0H	1	0	0	1
12	73	B1H ~ C3H	1	1	1	0
13	80	C4H ~ D2H	1	1	0	1
14	85	D3H ~ ECH	1	0	1	1
15	100	EDH ~ FFH	1	1	1	1

FIG. 8

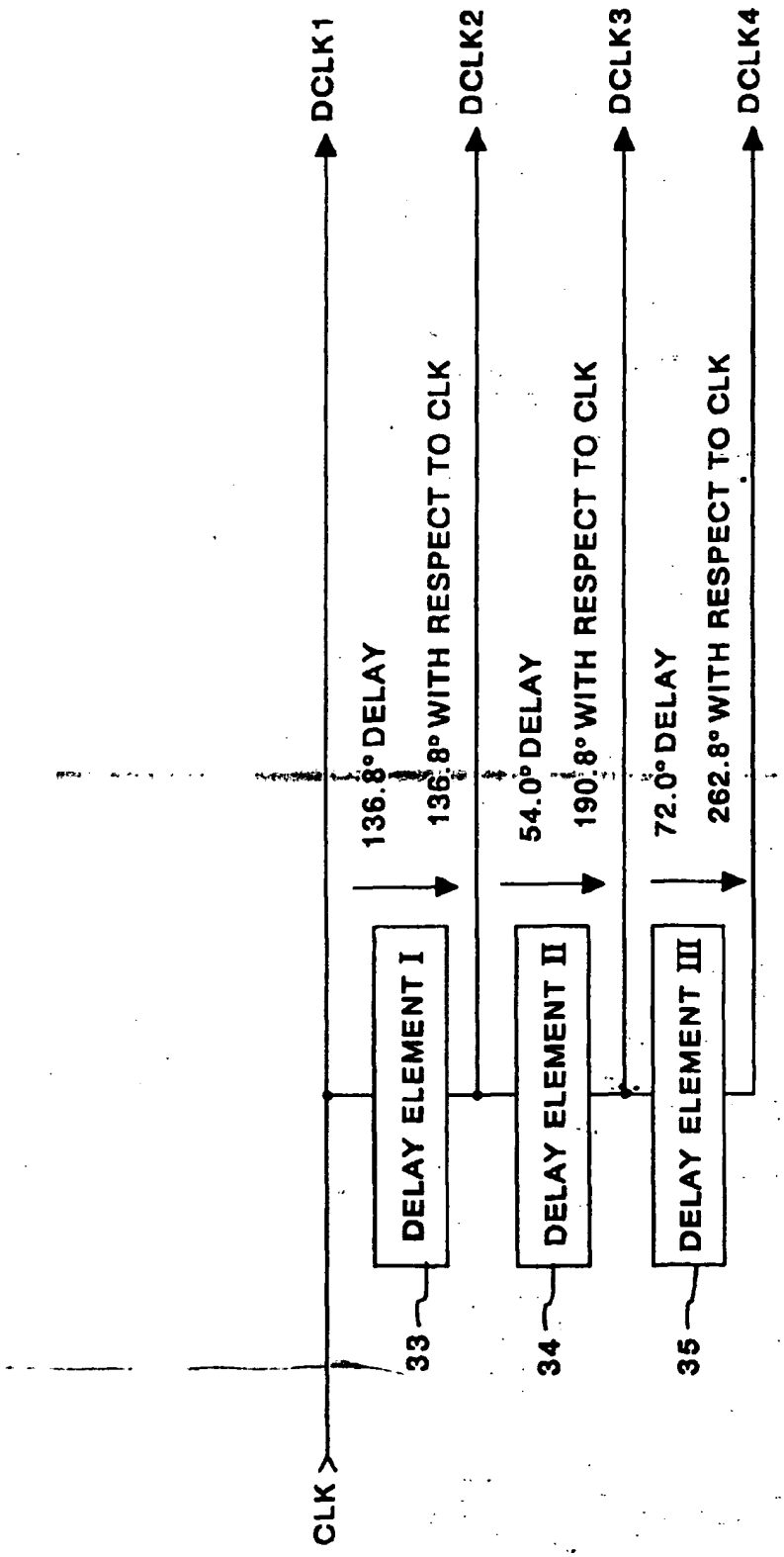
CLK
DCLK1
DCLK2
DCLK3
DCLK4
DELAY ELEMENT I
DELAY ELEMENT II
DELAY ELEMENT III
33
34
35
136.8° DELAY
136.8° WITH RESPECT TO CLK
54.0° DELAY
190.8° WITH RESPECT TO CLK
72.0° DELAY
262.8° WITH RESPECT TO CLK

FIG. 9

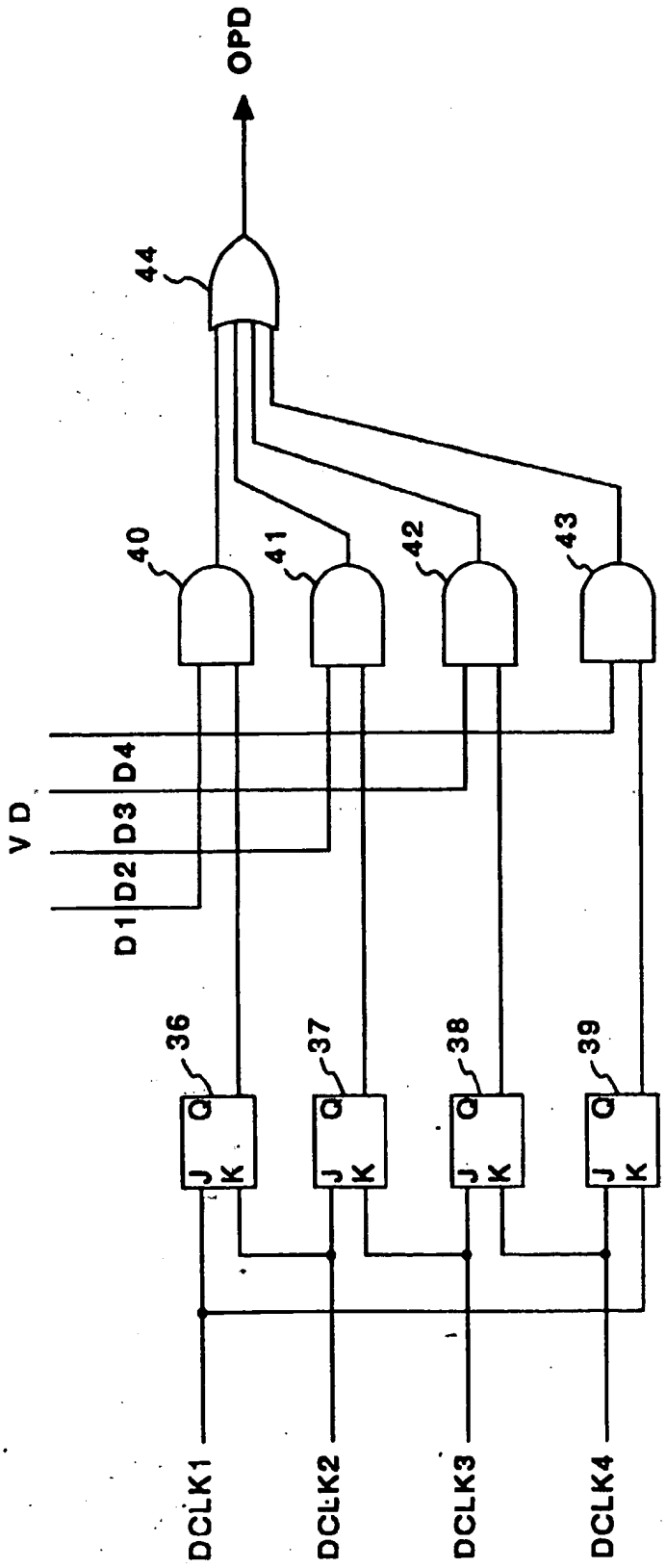
OPD
44
40
41
42
43
V D
D4
D3
D2
D1
36
37
38
39
Q
J
K
DCLK1
DCLK2
DCLK3
DCLK4

FIG. 10

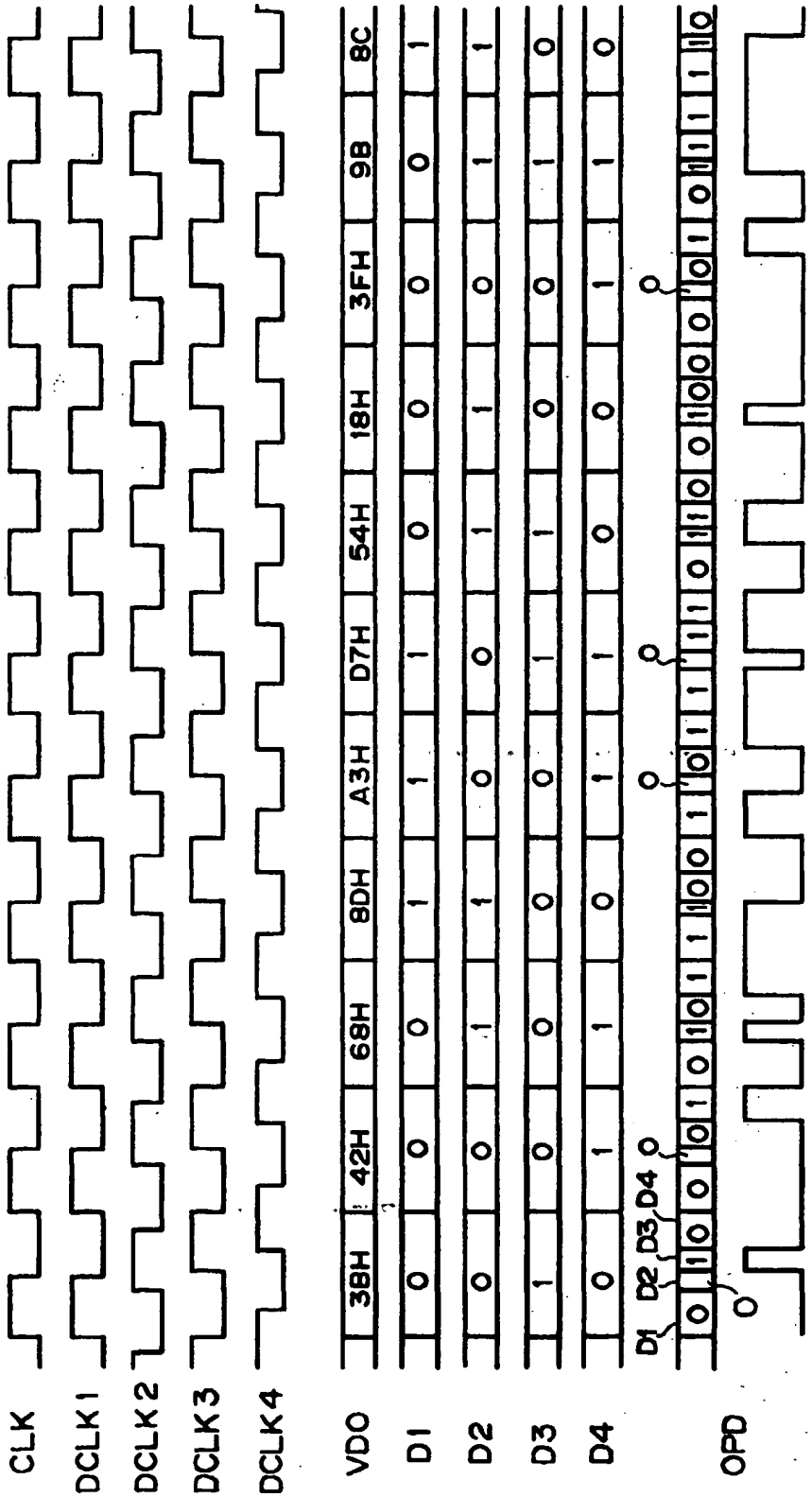
CLK
DCLK1
DCLK2
DCLK3
DCLK4
VDO
D1
D2
D3
D4
OPD
38H
42H
68H
8DH
A3H
D7H
54H
18H
3FH
9B
8C
D1
D2
D3
D4

FIG. 11

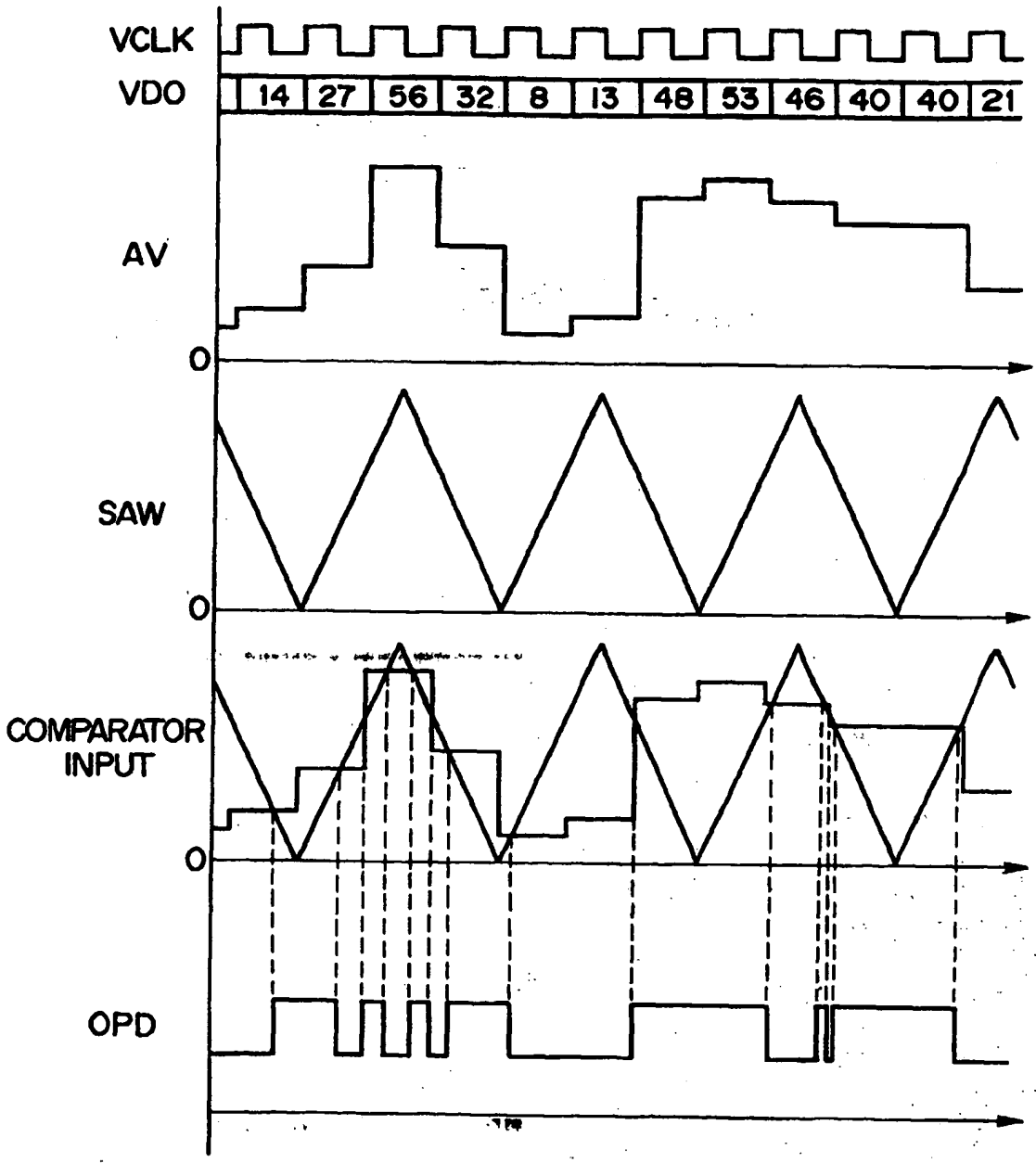
VCLK
VDO
14
27
56
32
8
13
48
53
46
40
40
21
AV
0
SAW
0
COMPARATOR INPUT
0
OPD

FIG. 12

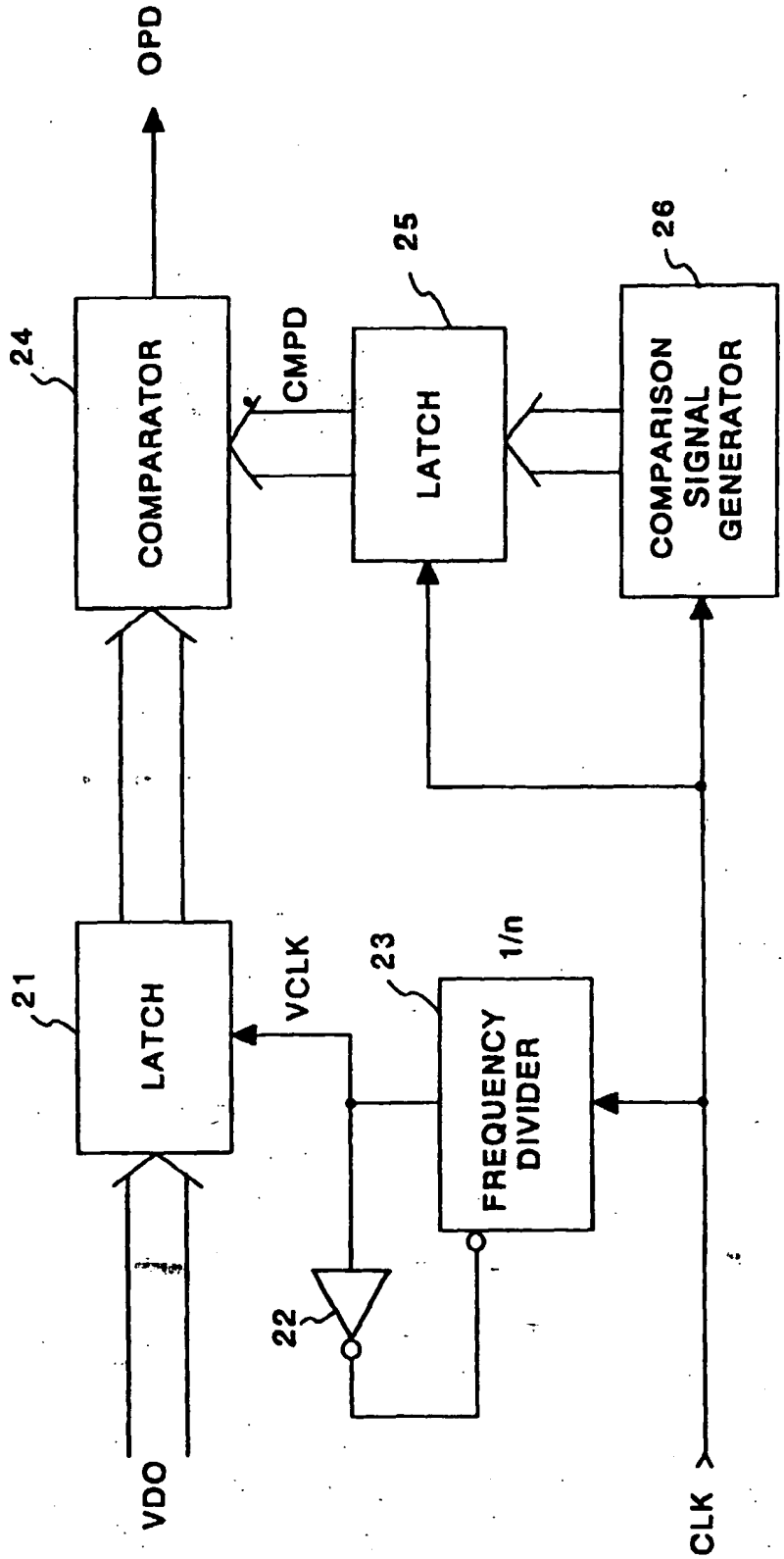
OPD
24
COMPARATOR
CMPD
25
LATCH
26
COMPARISON SIGNAL GENERATOR
21
LATCH
VCLK
23
1/n
FREQUENCY DIVIDER
22
VDO
CLK

FIG. 13

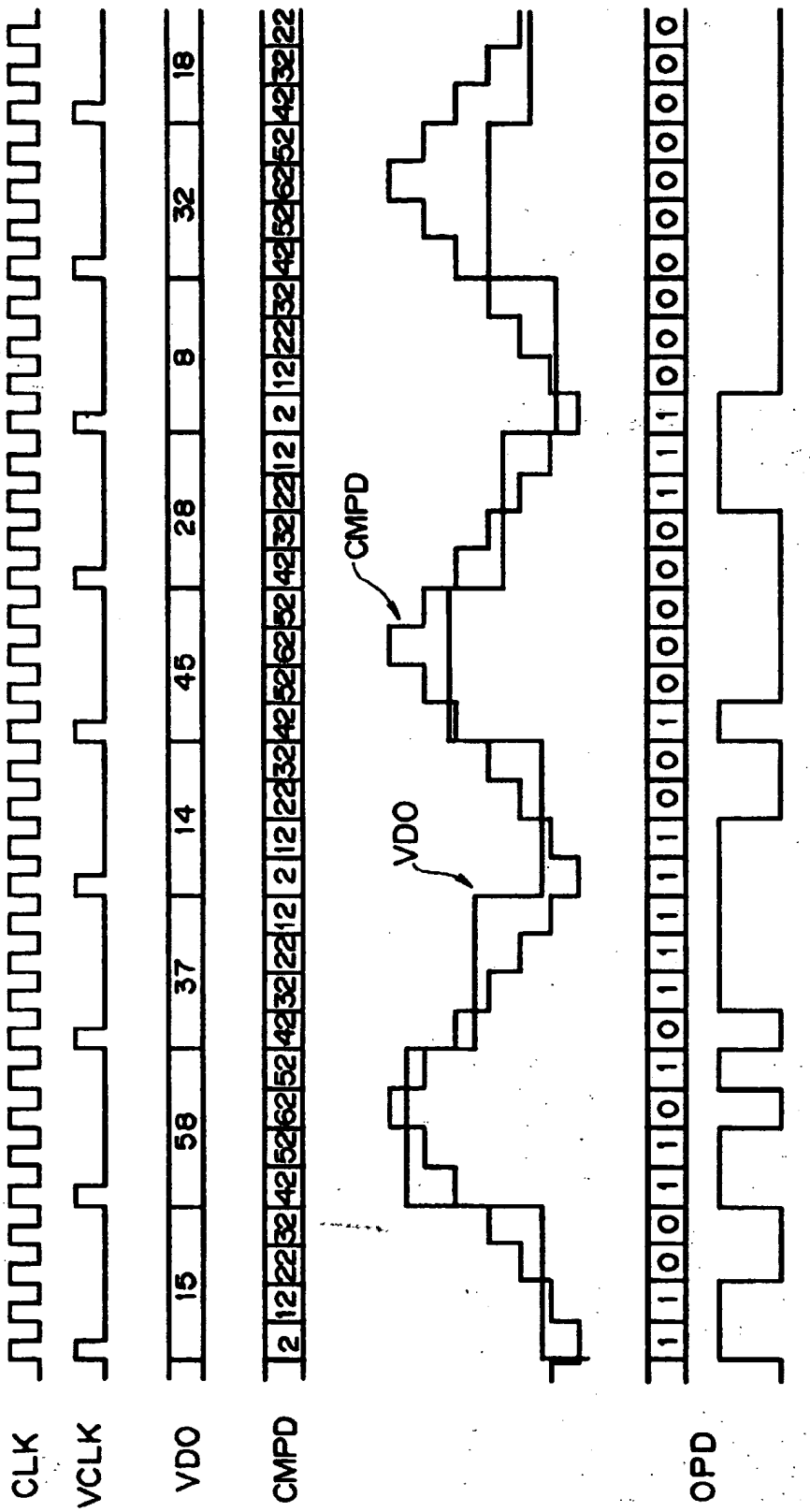

FIG. 14

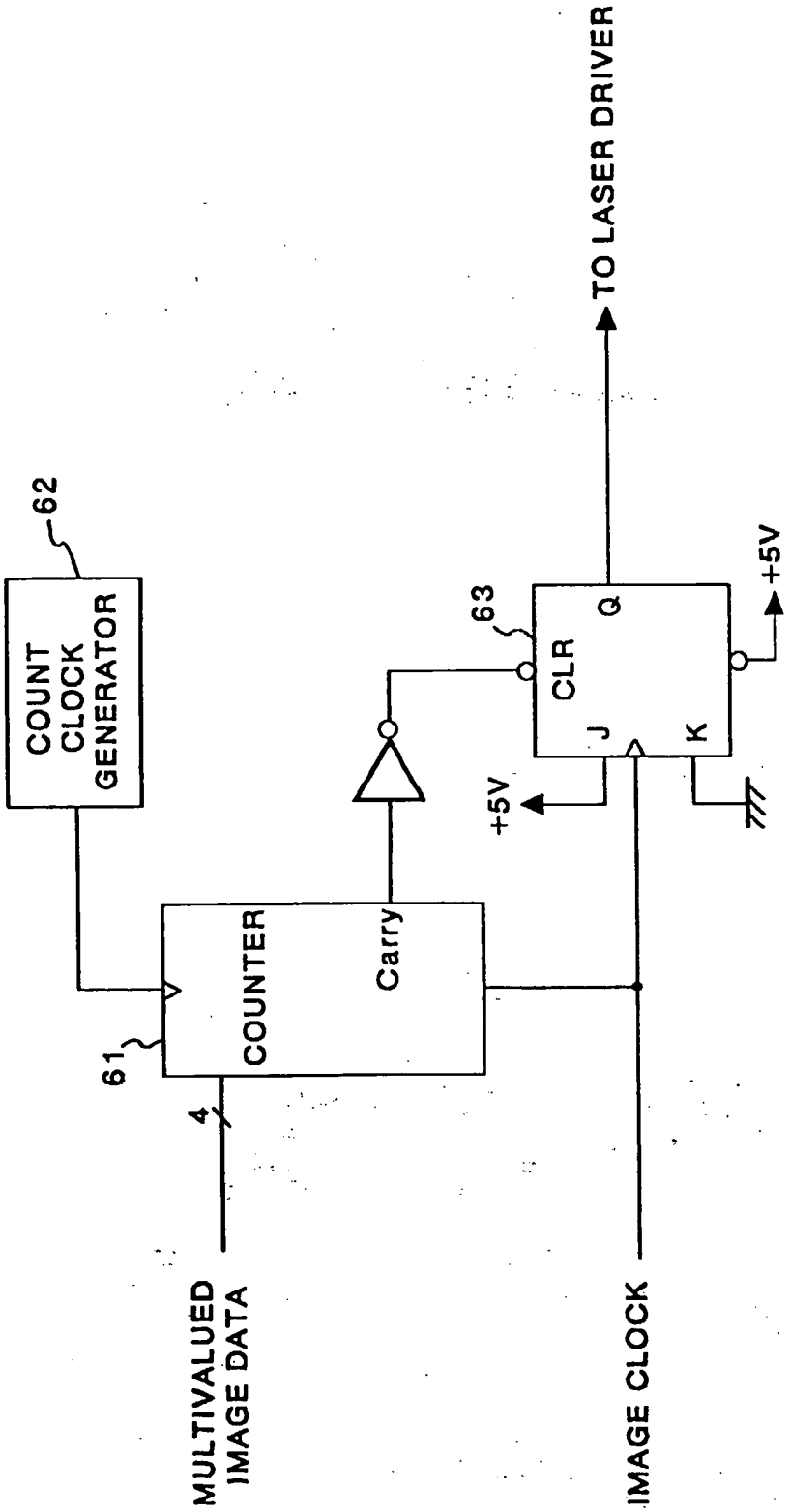
62
COUNT CLOCK GENERATOR
63
CLR
Q
J
K
+5V
+5V
TO LASER DRIVER
61
COUNTER
Carry
4
MULTIVALUED IMAGE DATA
IMAGE CLOCK

FIG. 15

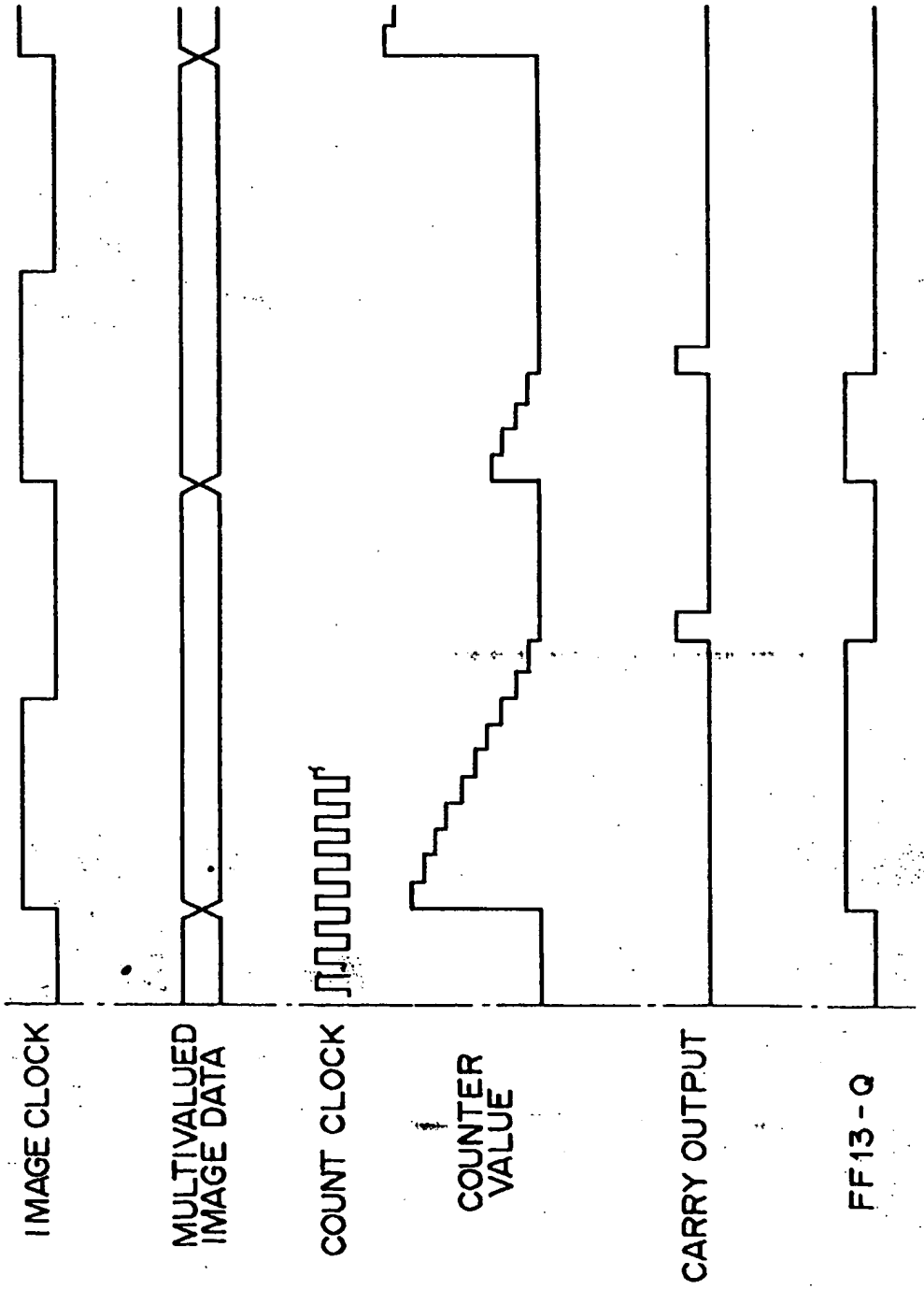
IMAGE CLOCK
MULTIVALUED IMAGE DATA
COUNT CLOCK
COUNTER VALUE
CARRY OUTPUT
FF13-Q

FIG. 16

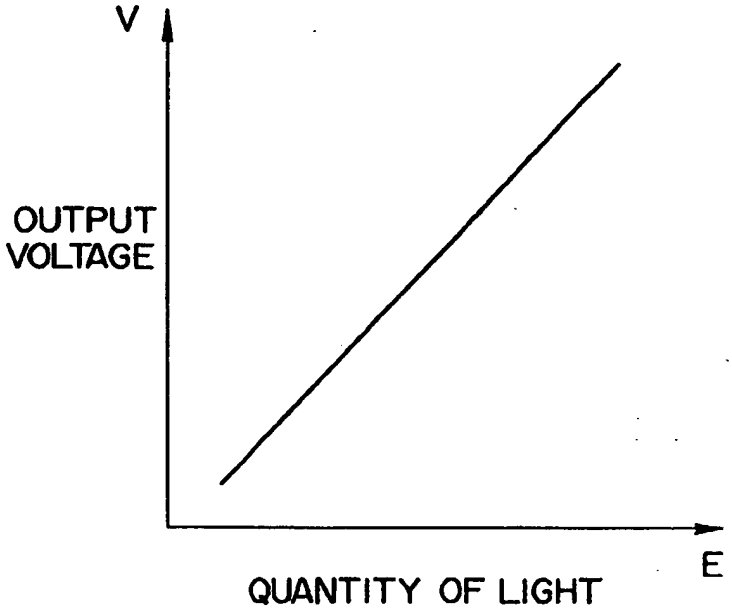

FIG. 17(a)

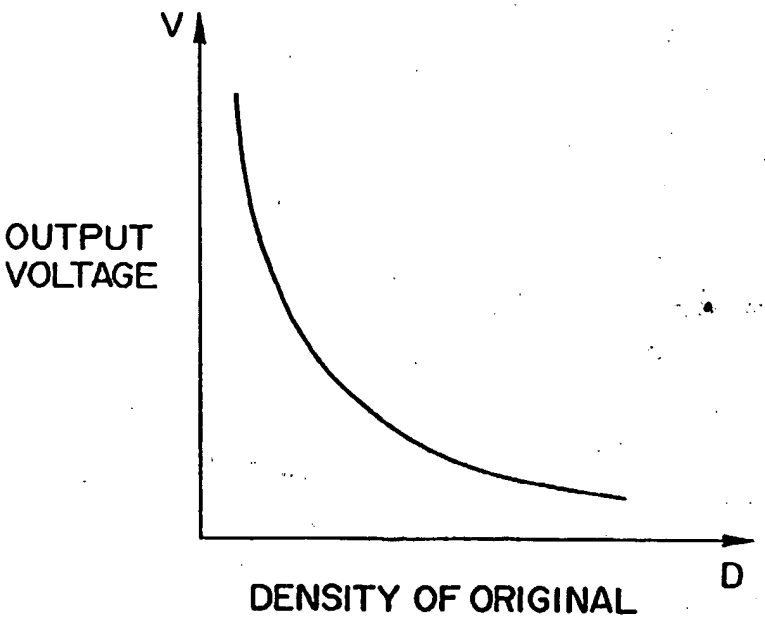

FIG. 17(b)